KAWA ELECTRONIC RESEARCH & DEVELOPMENT CENTRE

Service Manual

Reference No. : SM- LCT42AEAIA1CS-001
Revision : 0
Date : 2006.Dec.
Page : P.1 of 135

In House Model No. : LCT42AE
Customer Model No. : LCT42Z6TA

BOM No : LCT42AEAIA1CS -A01

Description : Service Manual for LCT42Z6TA _CMO_USA

Prepared By: 练沛珍

Checked By: Electronic Engineer 2006.12.7

Mechanical Engineer

Approved By: Engineering Manager

Received By: MK Department

DOC Rev NO.	The Latest Revision Details	DATE
0	Initial Release	2006-12-8

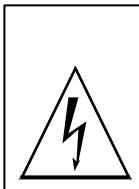
AKAI

SERVICE MANUAL

Model: LCT42Z6TA

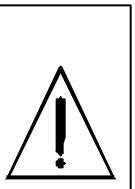
This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

I. Safety Instructions



CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN



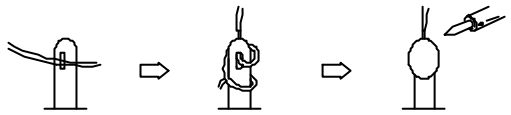
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated " dangerous voltage" within the product' s enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements. Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

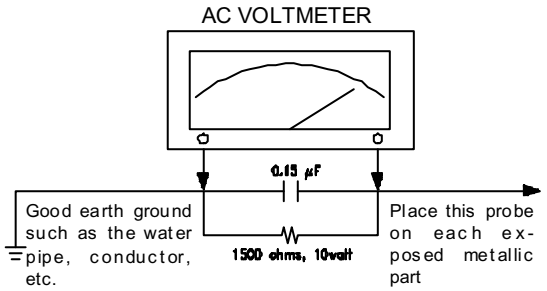
Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.
Please leave them at an appropriate depot.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.
   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15μF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time.
   Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.
   The measured voltage must not exceed 0.3V RMS. This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.
   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.

1.Do not power on .

1.1 Please check AC cable if connect to AC plug.

Is true the connector don’t connect to AC plug. Please connect it.

2.2 Please check AC cable if connect to AC power.

Is true the AC cable don’t connect to AC power. Please connect it.

3.3 Please check power board of fuse if broken.

If the F1 fuse is broken, Please pull out the AC cable from AC power. Please check AC L power and AC N ground by multimeter, The read number is infinite, the fuse is broke. then look up power board if not burn out place. Is true it. Please change power board or be changed power board.

2. The power on switch of green extinguish.

2.1 The power of led(indicator light) is red light, To touch power on key when indicator light wink.

Is true that the power DC output have somewhere short circuit.

Please check connector J6, J23 .If not connector direction is wrong.

Or the mainboard somewhere of power short circuit.

3.The power is normal work ,but don’t backlight.

3.1 The indicator light work normal (green light).

Please check Main board of transistor Q18 collect if not has +5v voltage.

Is true Q18 collect hasn’t +5v ,To check Q18 if fail. Or to check Q18 of base if not low. (Low is working, high don’t work).

Please refer to attached sheet A circuit diagram.

3.2 Please check backlight of connector if not it direction is wrong or the connector of wire compositor direction is wrong.

3.3 To check connector panel of voltage is +24v. It’s true .Then to check of the first pin if it have +5V voltage, It’s true , than to check power board of +24v voltage ,It’s true. The panel of backlight board is fail. The change panel of backlight board.

Please refer to attached sheet B Panel of datasheet.

4.The screen don’t have picture But have backlight.

4.1 To check to panel of voltage ,To check main board of bead L69 and L57 connect if not OK.Then check the L69 and L57 of voltage is +12v(27 inch panel voltage is +5v, To check L68 and L56) . Next to check fuse F1 and connector J10 if not is +12v(27 inch panel voltage is +5v). If isn’t please check power board of connector CON5 if has +12v(27 inch panel voltage is +5v).

4.2To check to main board +12 V voltage. To check to main board IC U35 of the first pin if

+5v voltage ,It’s fail. It’s low (close 0 v) working.

The circuit diagram follow down:

Please refer to attached sheet A circuit diagram.

5.The remote control don’t be control.

6.1 The check batteries of remote control if it run out of .

6.2 To check main board of connecter J21 of wire connect fastness and the connecter of wire open.

Please refer to attached sheet A circuit diagram.

6.The sound don’t output.

7.1 To check main board +24v voltage of connector J39, It’s true not +24v voltage. Then to check power main +24v fail .

Please refer to attached sheet A circuit diagram.

7.The DTV don’t detect .

7.1 To check mainboard of connecter J24 and DTV mainboard of connector HA1 of FCC wire if no connect fastness.

Please refer to attached sheet C of DTV circuit diagram.

Product Specification

Product Model	LCT42Z6TA
TV System	NTSC M, ATSC
VIDEO System	NTSC
Screen Size	42” diagonal
Display Area	930.24mm (W) x 523.26mm (H)
Aspect Ratio	16:9
External Size (with stand)	1067.3mm (W) x 781.2mm (H) x 275mm (D)
Net Weight (with stand)	27.5 kg
Display Resolution	1920(H) x 1080(V) Pixels (Each pixel has R/G/B 3 color cells)
Pixel Dot Pitch	0.4845 (H) x 0.4845 (V) mm
Color	16.7 millions of colors (R/G/B each 256 scales)
Gray Scale	256 (R/G/B each 8-bit)
Brightness (Peak)	500cd/m^2
Contrast (Dark Room)	800:1
Sound Effect	Acoustic Cinema Enhancement
Power Supply	AC 120V, 60 Hz
Power Consumption	300W
Input Terminal	Antenna Input (F Type) x 2 (NTSC&ATSC)
	RS-232(D-SUB 9 Pin Type) x 1 (only for ATSC)
	HDMI (Ver. 1.1) connector x 1
	VGA (D-Sub 15 Pin Type) x 1
	Component Video - YPbPr x 2 RCA Terminals
	Video Input RCA Terminals x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 5
Output Terminal	1 set of Audio Output Terminals (RCA, L&R)

Note: The specifications shown above may be changed without notice for quality improvement.

Support the Signal Mode

A. VGA Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
	37.86	72.81
800 x 600	35.16	56.25
	37.90	60.32
	46.90	75.00
	48.08	72.19
1024 x 768	48.40	60.00

B. YPbPr Mode

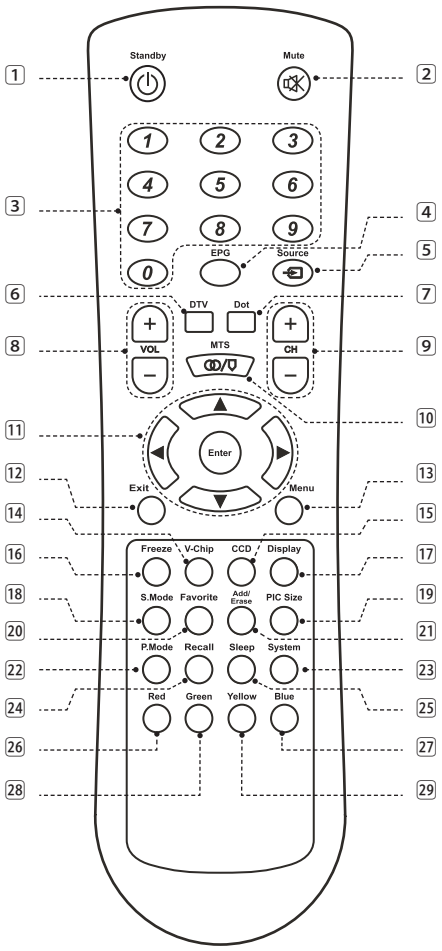
Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480i	15.734	59.94
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00
1080P(1920x1080)	67.50	60.00

C. HDMI Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00
1080P(1920x1080)	67.50	60.00

- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.

Remote Control



1. **Standby(⏻):** Press this button to turn off to standby and turn on from standby.
2. **Mute(🔇):** Press this button to quiet the sound system. Press again to reactivate the sound system.
3. **0~9 Number Buttons**: Press 0~9 to select a channel, and used to input the password; the channel changes after 2 seconds.
4. **EPG (Electronic Program Guide)**: Press to display EPG mode. Press again to exit EPG mode.
5. **Source**: Press to select the signal source, such as DTV, TV, AV, S-Video, YPbPr 1, YPbPr 2, VGA or HDMI.
6. **DTV**: Press to choose DTV directly.
7. **Dot:** Press number buttons with it to select the channels directly in DTV.
8. **VOL +/-**: Press to adjust the volume.
9. **CH +/-** : Press to select the channel forward or backward.
10. **MTS**: Press repeatedly to cycle through the Multi-channel TV sound (MTS) options: Mono, Stereo and SAP (Second Audio Program).
11. ◄,►,▲,▼, **Enter**: Press ◄, ►, ▲, ▼ to move the on-screen cursor. To select an item, press **Enter** to confirm.
12. **Exit**: Press this button to exit.
13. **Menu**: Press to enter into the on-screensetup menu, press again to exit.
14. **V-Chip**: Press to select the child protect mode.
15. **CCD**: Press to select the Closed Caption mode.
16. **Freeze**: Press to freeze the picture, press again to restore the picture. (inactive for 1080i (1920x1080) in YPbPr).
17. **Display**: Press to display the channel information and it disappear after 3 seconds.
18. **S. Mode**: Press repeatedly to select the sound mode: Normal, News, Cinema, Concert and User.
19. **PIC Size**: Press repeatedly to cycle through the picture size. when in DTV, YPbPr1, YPbPr2 mode, it can select picture size is: Full, 4:3. While in other mode, it can select picture size is: Full, 4:3, Panoramic.(Note: when in VGA mode, it can only select “Full”.)
20. **Favorite**: Press repeatedly to cycle through the favorite channel list.
21. **Add/Erase**: Press to add or delete favorite or dislike channels.
22. **P. Mode**: Press repeatedly to cycle through the picture mode: Cinema, Normal, Vivid, Hi-Bright and User.
23. **System**: Press repeatedly to cycle through the system options: AUTO, NTSC 3.58 and PAL. (Only for AV or S-Video)
24. **Recall**: Press to return to previous channel.
25. **Sleep**: Press repeatedly until it displays the time in minutes (15 Min, 30 Min, 60 Min, 90 Min, 120 Min and, Off) that you want the TV to remain on before shutting off. To cancel sleep time, press Sleep button repeatedly until sleep Off appears.
26. **Red**: Press this button to access the red item or page.
27. **Blue**: Press this button to access the blue item or page.
28. **Green**: Press this button to access the green item or page.
29. **Yellow**: Press this button to access the yellow item or page.

Optical Output

Flash 32mb

MT5351 MPEG Decoder

DDR 256M

DDR 256M

TD1336 Digital Tuner

X6965D SAW Filter

MT5111 DTV Demodulator

DTV BOARD

POWER BOARD

5V

Standby 5V

12V

9V

24VA (For Class D)

24V (For LCD Panel)

MAIN BOARD

HDMI

MT8293 HDMI Receiver

74L VC245A X4 24 bit RGB Switch

Analog Tuner

To panel

YPbPr1

YPbPr2 (Option)

QS3VH257 Switch(Option)

MT8206 ADC & Scaler & LVDS Transfer

Flash 8M/16M

VGA

NJRC4558 Audio Buffer

Audio Output

AV

DDR 128M

S-Video

DDR 128M

Audio X2

HEF4052 Switch

WM8776 Audio ADC&DAC

Max232 Level Shift

RS232 Socket

Audio X3

R2S15102 Class D Amplifier

Relay

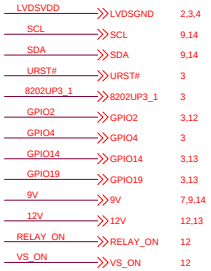
Speaker

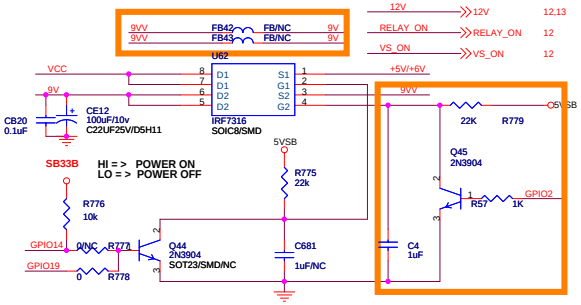
LCD panel

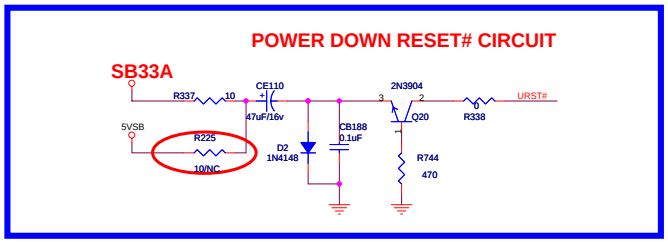
MT8202E (PBGA388) LCDTV BOARD 4 LAYERS FOR AKAI

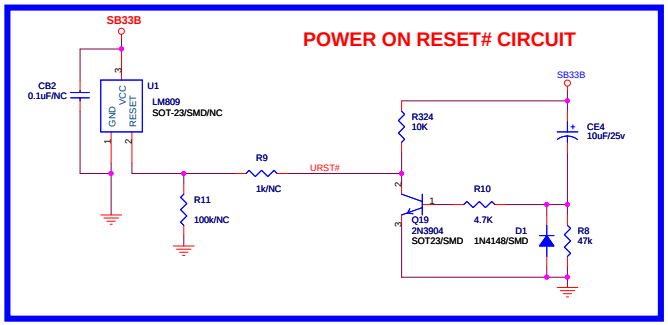
1. INDEX / POWER / RESET / EEPROM
2. LDO
3. MT8202E PBGA388
4. MT8202 DECOUPLING
5. DDR MEMORY & FLASH
6. MT5351 INTERFACE
7. HDMI MT8293
8. DAUGHTER BOARD IN
9. WM8776 & VIDEO BYPASS
10. AUDIO / VIDEO IN CIRCUIT
11 . VGA & PC AUDIO IN
12. LVDS OUT
13. BACK LIGHT / KEYPAD
14. TUNER IN
15. AV IN
16. AUDIO IN
17.AUDIO Amplifier

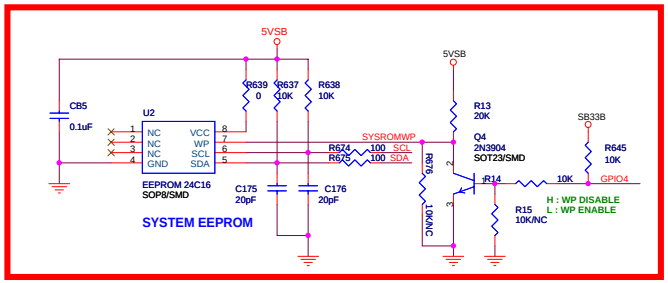
Rev	History	P#	Date
AKAI_MT8202_27US_LVDS_V0.0	New		2005/11/22
AKAI_MT8202_27US_HDMI_LVDS_V0.0	ADD HDMI / VIDEO /AUDIO CONNECTOR INPUT IN		

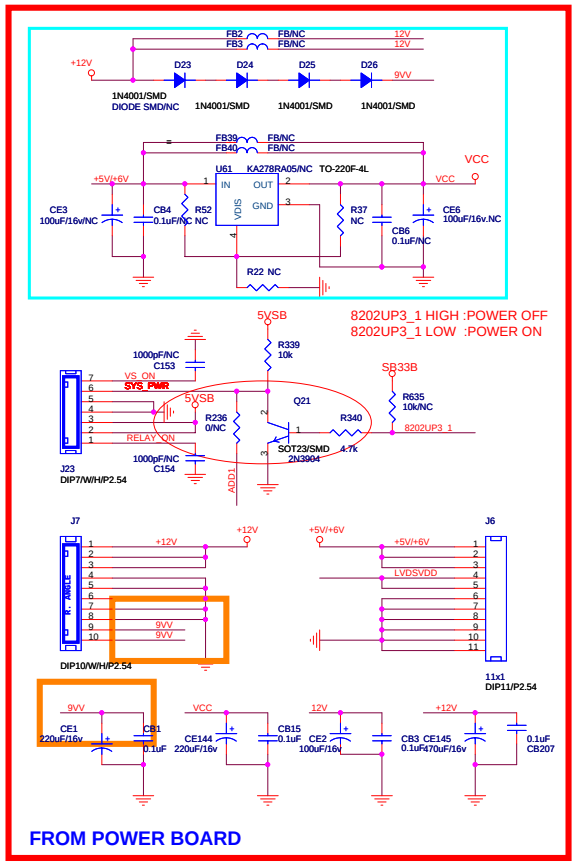


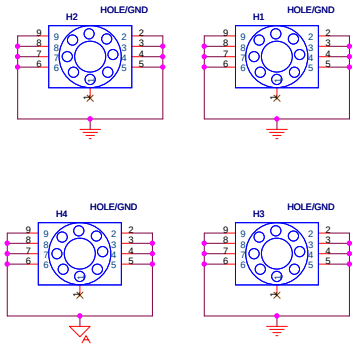






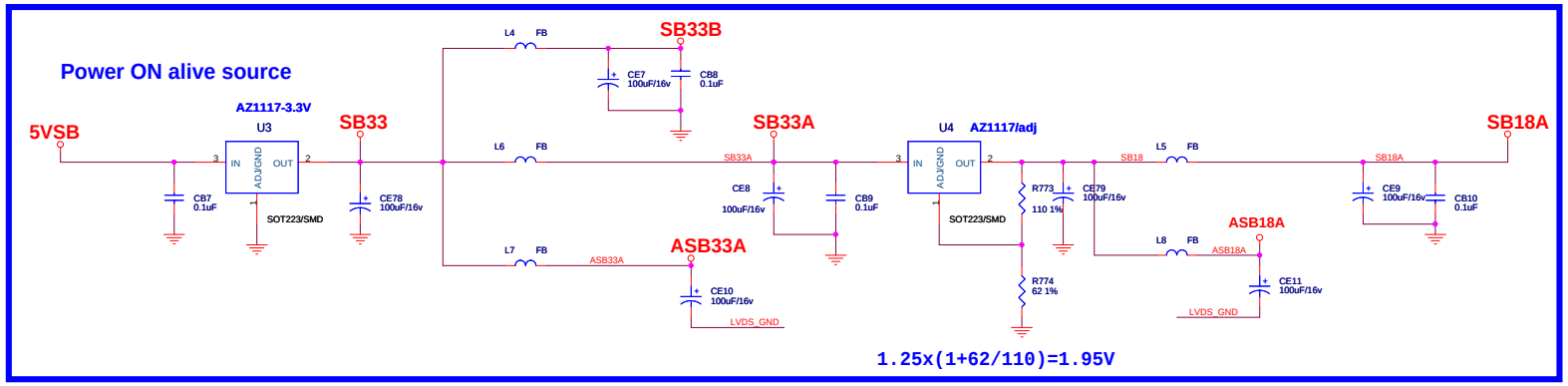


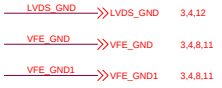


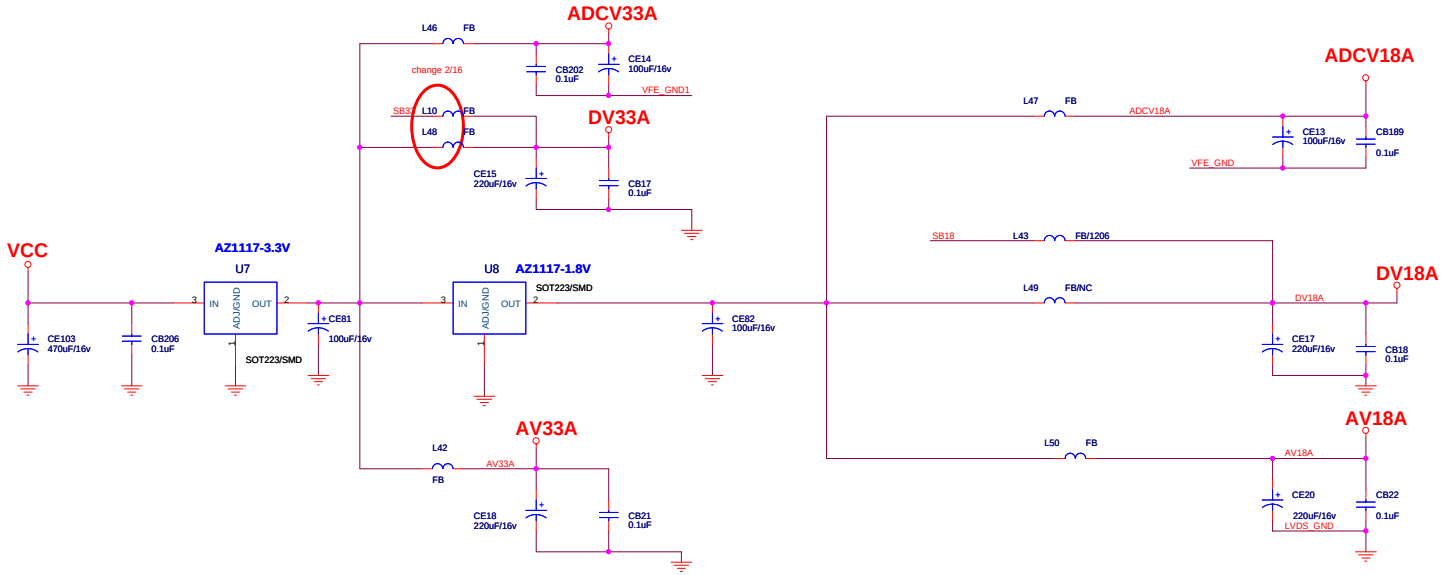


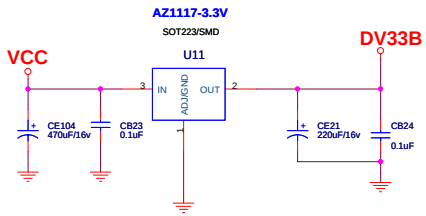
KAWA Confidential

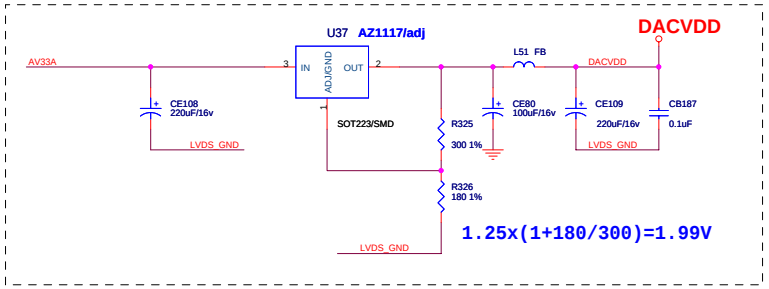
Title: INDEX / POWER / RESET / EEPROM			
Size: C	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, April 13, 2006		Sheet 1	17





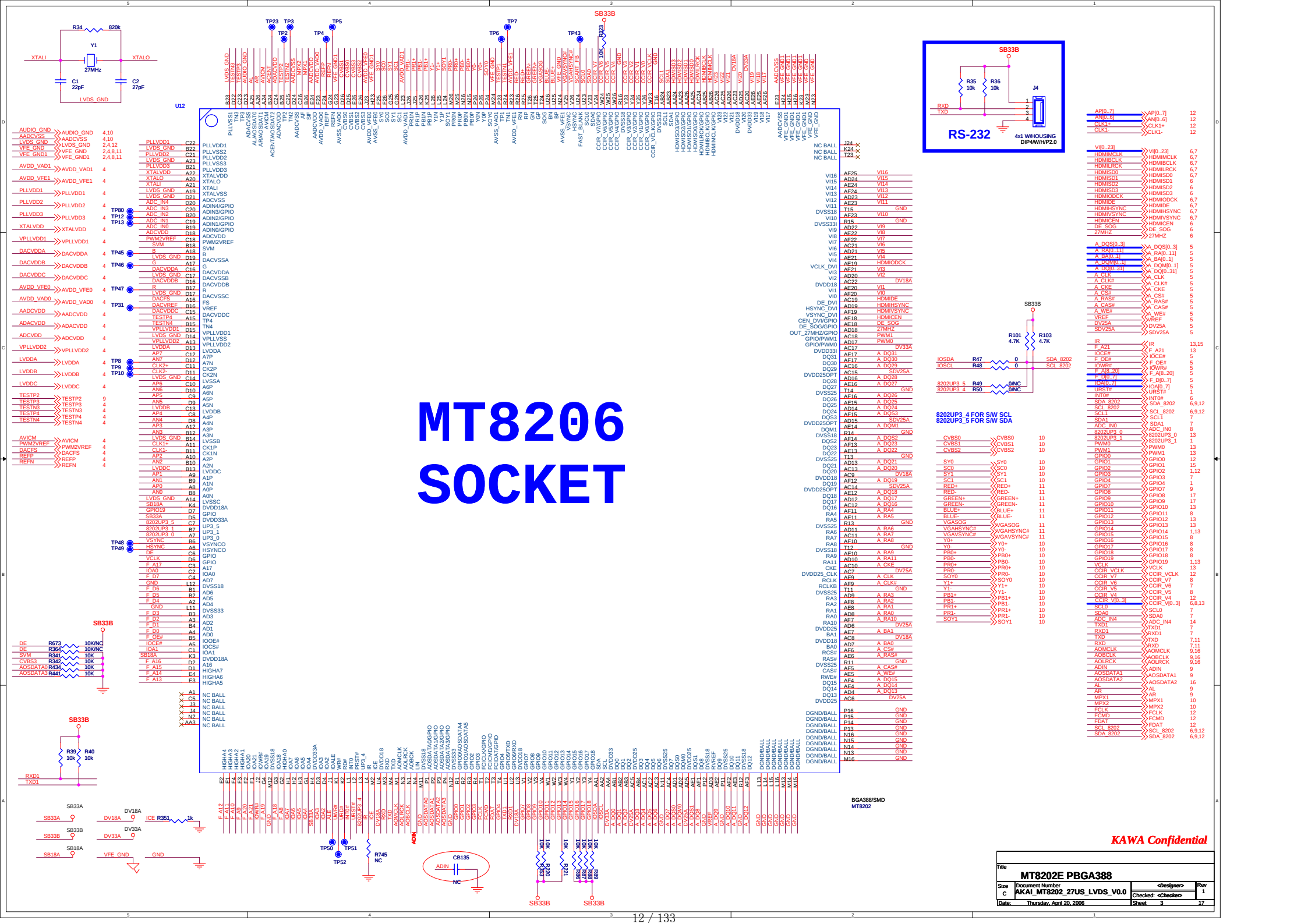






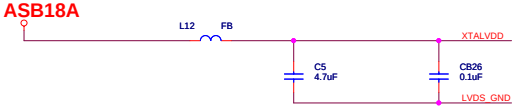
KAWA Confidential

Title: LDO			
Size: C	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer> / Checked: <Checker>	Rev: 1
Date: Thursday, April 13, 2006		Sheet 2	17

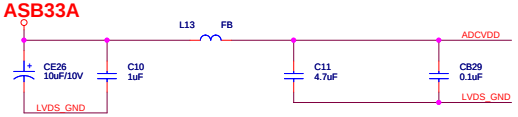

MT8206
SOCKET
U12
SB33B
RS-232
4x1 W/HOUSING
DIP4/W/H/P2.0
KAWA Confidential
MT8202E PBGA388
AKAI_MT8202_27US_LVDS_V0.0
Thursday, April 20, 2006
BGA388/SMD
MT8202

STANDBY ANALOG POWER

ASB18A

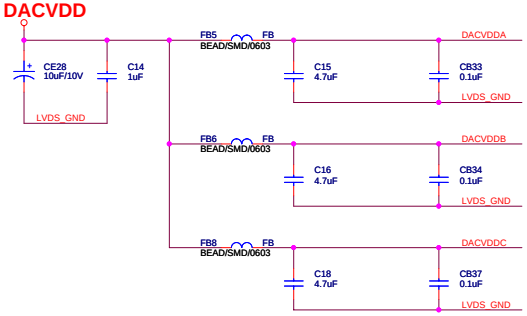


ASB33A



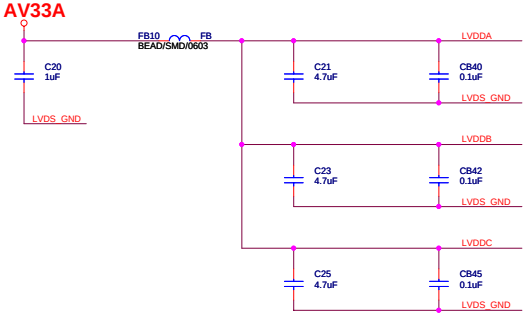
NORMAL VIDEO DAC POWER

DACVDD



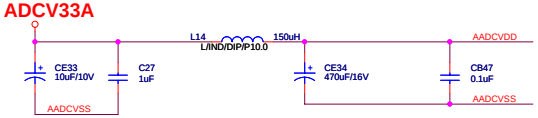
NORMAL VIDEO DAC POWER

AV33A

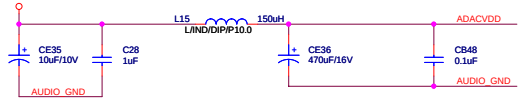


NORMAL AUDIO ADC / DAC POWER

ADCV33A

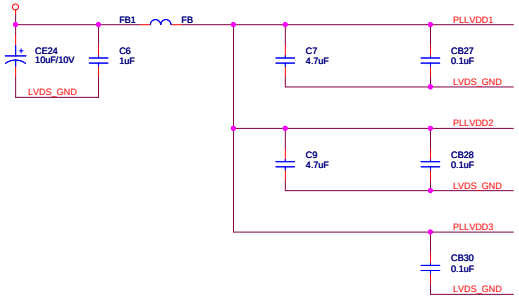


ADCV33A

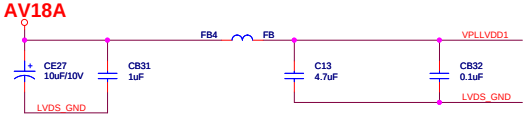


NORMAL ANALOG POWER

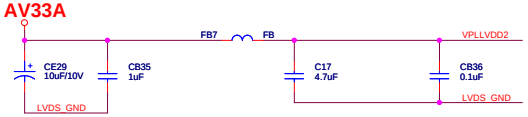
ASB18A



AV18A

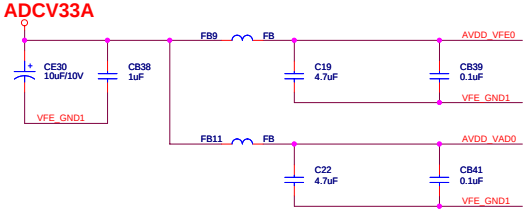


AV33A

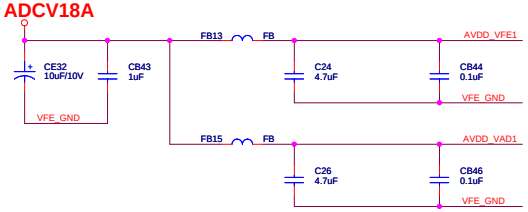


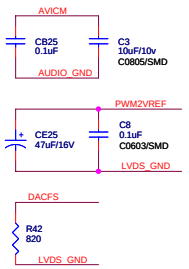
NORMAL VIDEO ADC POWER

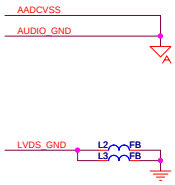
ADCV33A

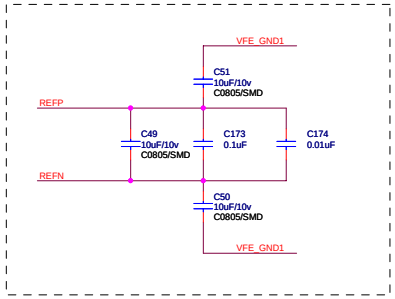


ADCV18A



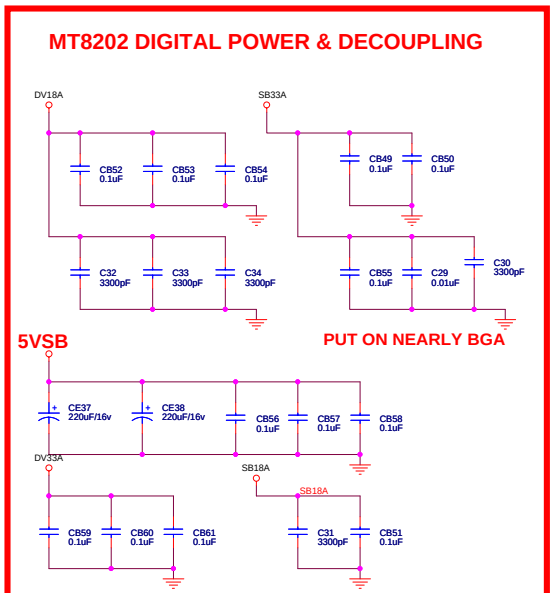






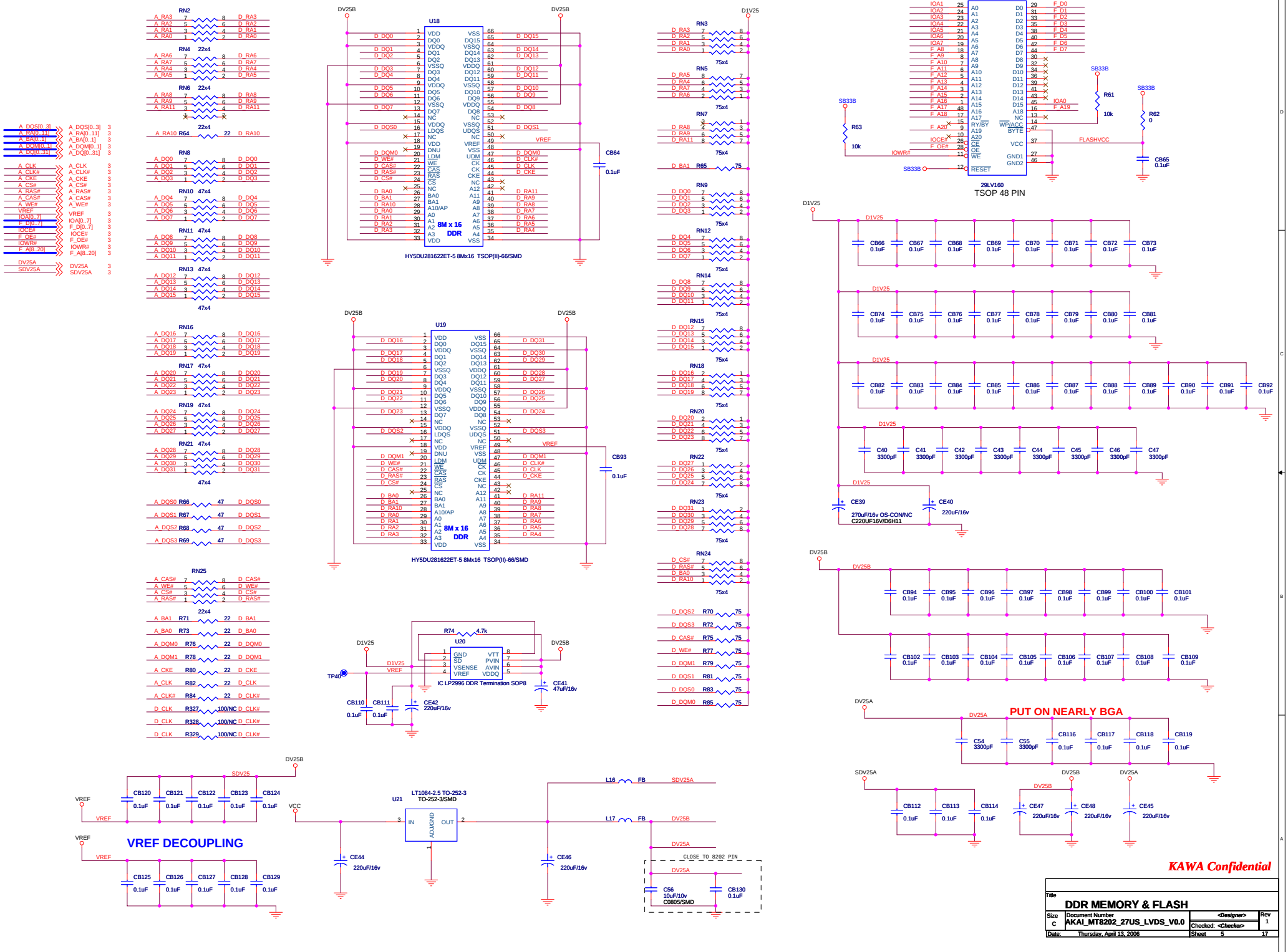
TESTP3	R43	49.9 1%	PLLVDD1
TESTN3	R44	49.9 1%	PLLVDD1
TESTP4	R45	49.9 1%	VPLLVDD1
TESTN4	R46	49.9 1%	VPLLVDD1

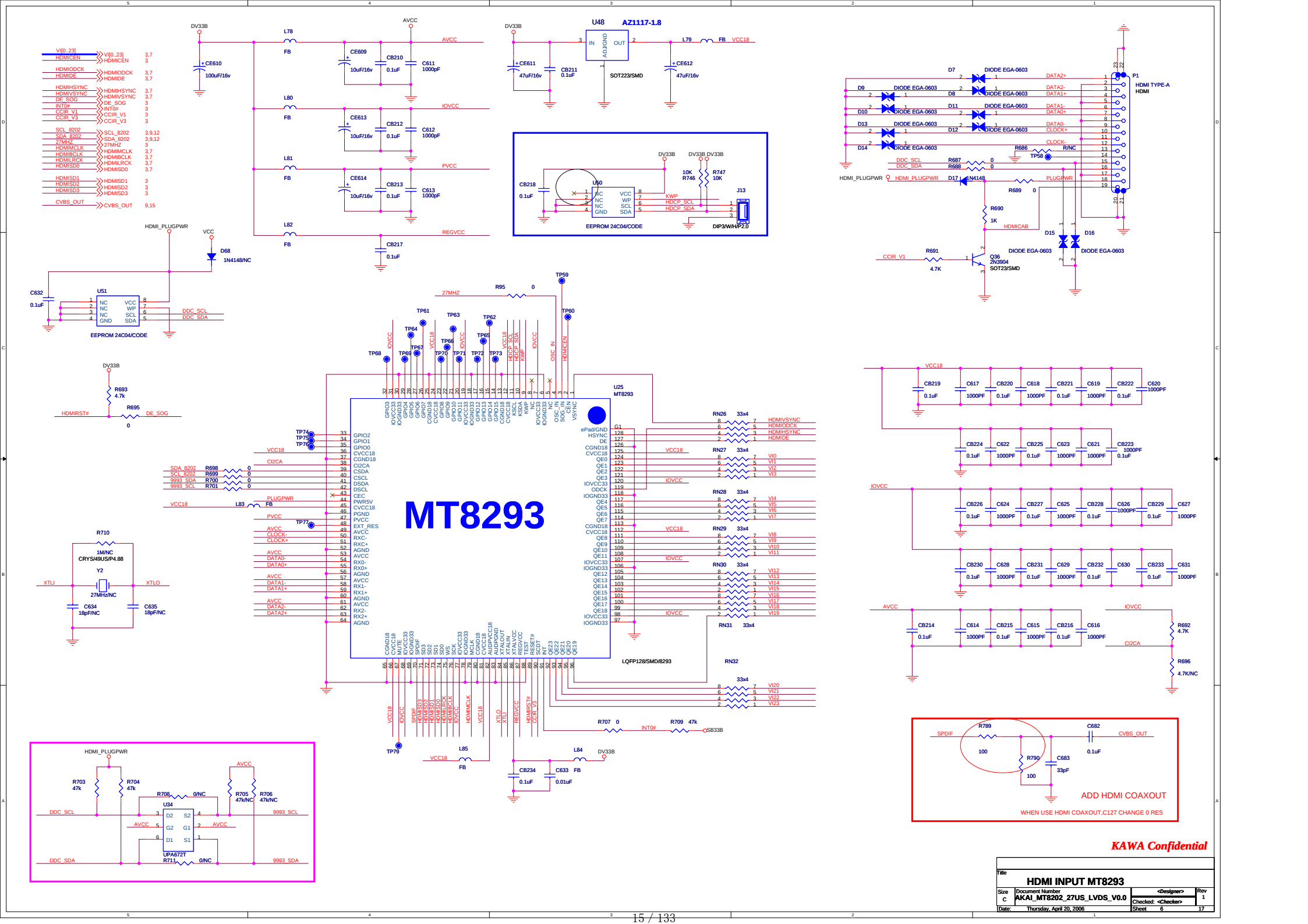
MT8202 DIGITAL POWER & DECOUPLING

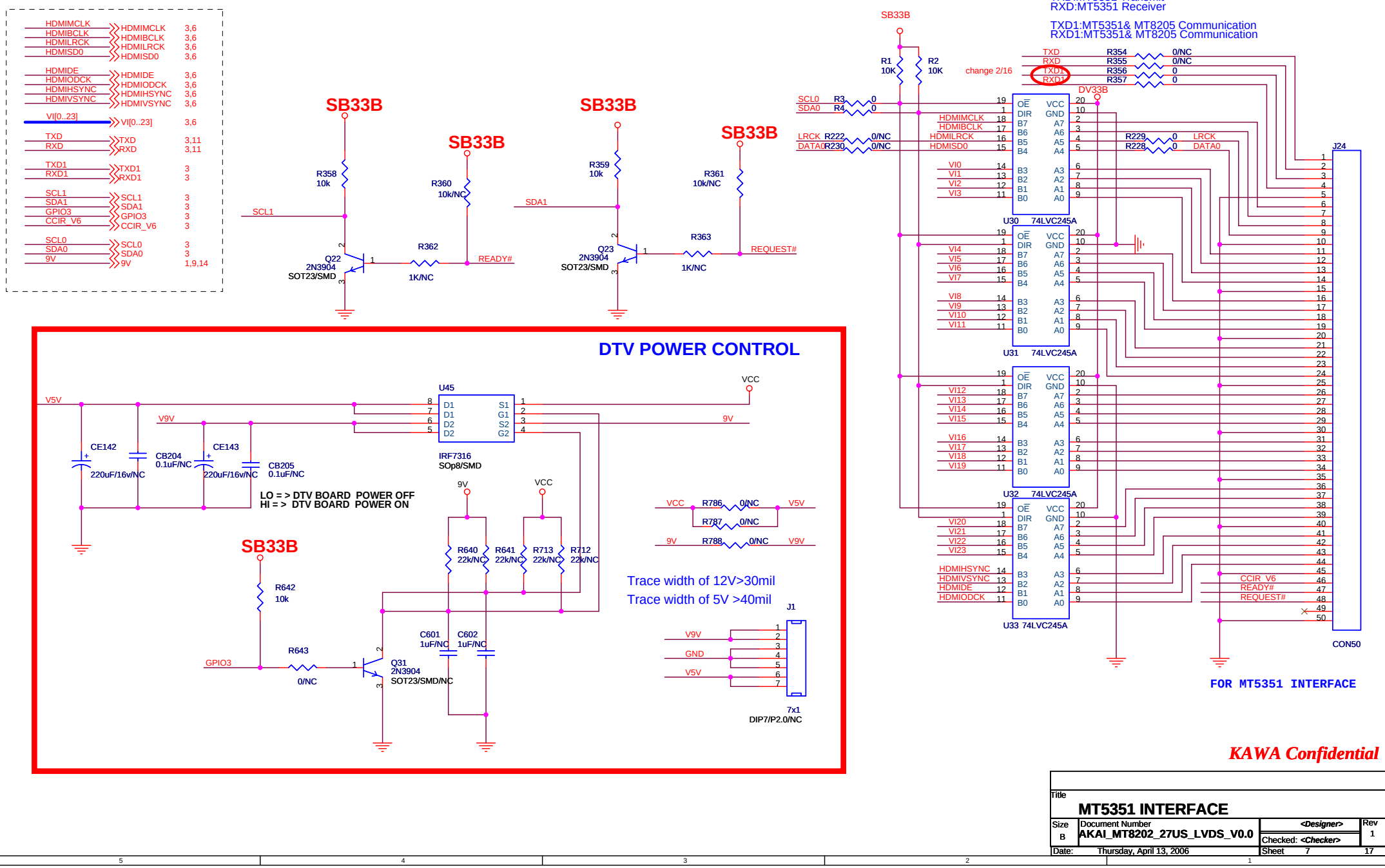


KAWA Confidential

Title	MT8202 DECOUPLING		
Size C	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev 1
		Checked: <Checker>	
Date: Thursday, April 13, 2006		Sheet 4	17


RN2
RN4 22x4
RN6 22x4
RN8
RN10 47x4
RN11 47x4
RN13 47x4
RN16
RN17 47x4
RN19 47x4
RN21 47x4
RN25
R64 22
R66 47
R67 47
R68 47
R69 47
R71 22
R73 22
R76 22
R78 22
R80 22
R82 22
R84 22
R327 100/NC
R328 100/NC
R329 100/NC
U18
HY5DU281622ET-5 8Mx16 TSOP(II)-66/SMD
U19
HY5DU281622ET-5 8Mx16 TSOP(II)-66/SMD
8M x 16 DDR
R74 4.7k
U20
IC LP2996 DDR Termination SOP8
TP40
CB110 0.1uF
CB111 0.1uF
CE42 220uF/16v
CE41 47uF/16v
CB64 0.1uF
CB93 0.1uF
RN3
RN5
RN7
RN9
RN12
RN14
RN15
RN18
RN20
RN22
RN23
RN24
R65 75
R70 75
R72 75
R75 75
R77 75
R79 75
R81 75
R83 75
R85 75
U17
29LV160
TSOP 48 PIN
R61 10k
R62 0
R63 10k
CB65 0.1uF
C66 0.1uF
C67 0.1uF
C68 0.1uF
C69 0.1uF
C70 0.1uF
C71 0.1uF
C72 0.1uF
C73 0.1uF
C74 0.1uF
C75 0.1uF
C76 0.1uF
C77 0.1uF
C78 0.1uF
C79 0.1uF
C80 0.1uF
C81 0.1uF
C82 0.1uF
C83 0.1uF
C84 0.1uF
C85 0.1uF
C86 0.1uF
C87 0.1uF
C88 0.1uF
C89 0.1uF
C90 0.1uF
C91 0.1uF
C92 0.1uF
C40 3300pF
C41 3300pF
C42 3300pF
C43 3300pF
C44 3300pF
C45 3300pF
C46 3300pF
C47 3300pF
CE39 270uF/16v OS-CON/NC C220UF16V/D6H11
CE40 220uF/16v
CB94 0.1uF
CB95 0.1uF
CB96 0.1uF
CB97 0.1uF
CB98 0.1uF
CB99 0.1uF
CB100 0.1uF
CB101 0.1uF
CB102 0.1uF
CB103 0.1uF
CB104 0.1uF
CB105 0.1uF
CB106 0.1uF
CB107 0.1uF
CB108 0.1uF
CB109 0.1uF
PUT ON NEARLY BGA
C54 3300pF
C55 3300pF
CB116 0.1uF
CB117 0.1uF
CB118 0.1uF
CB119 0.1uF
CB112 0.1uF
CB113 0.1uF
CB114 0.1uF
CE47 220uF/16v
CE48 220uF/16v
CE45 220uF/16v
CB120 0.1uF
CB121 0.1uF
CB122 0.1uF
CB123 0.1uF
CB124 0.1uF
CB125 0.1uF
CB126 0.1uF
CB127 0.1uF
CB128 0.1uF
CB129 0.1uF
VREF DECOUPLING
LT1084-2.5 TO-252-3
TO-252-3/SMD
U21
CE44 220uF/16v
CE46 220uF/16v
L16 FB
L17 FB
CLOSE TO 8202 PIN
C56 10uF/10v C0805/SMD
CB130 0.1uF
KAWA Confidential
DDR MEMORY & FLASH
AKAI_MT8202_27US_LVDS_V0.0
Thursday, April 13, 2006


MT8293
U25
MT8293
LQFP128/SMD/8293
U48
AZ1117-1.8
SOT223/SMD
U50
EEPROM 24C04/CODE
DIP3/W/HP2.0
U51
EEPROM 24C04/CODE
U34
UPA672T
P1
HDMI TYPE-A
HDMI
Q36
2N3904
SOT23/SMD
ADD HDMI COAXOUT
WHEN USE HDMI COAXOUT,C127 CHANGE 0 RES
KAWA Confidential
HDMI INPUT MT8293
Document Number
AKAI_MT8202_27US_LVDS_V0.0
Rev
1
Date: Thursday, April 20, 2006
Sheet 6 17

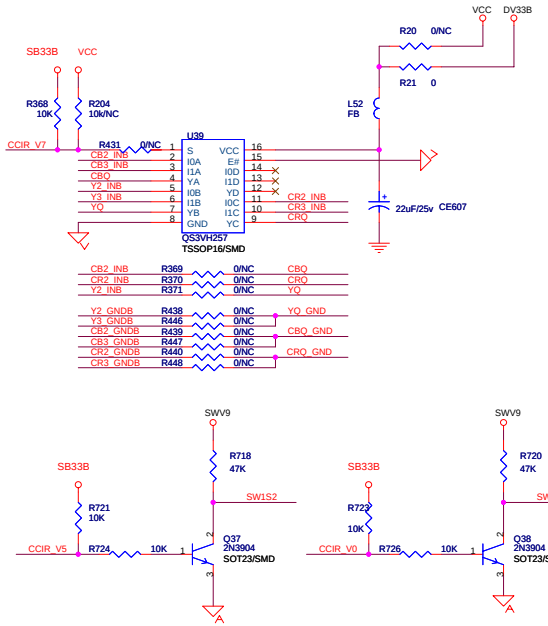

HDMIMCLK 3,6
HDMIBCLK 3,6
HDMILRCK 3,6
HDMISD0 3,6
HDMIDE 3,6
HDMIODCK 3,6
HDMIHSYNC 3,6
HDMIVSYNC 3,6
VI[0..23] 3,6
TXD 3,11
RXD 3,11
TXD1 3
RXD1 3
SCL1 3
SDA1 3
GPIO3 3
CCIR_V6 3
SCL0 3
SDA0 3
9V 1,9,14
SB33B
R358 10k
R360 10k/NC
SCL1
Q22 2N3904 SOT23/SMD
R362
1K/NC
READY#
R359 10k
SDA1
Q23 2N3904 SOT23/SMD
R363
1K/NC
R361 10k/NC
REQUEST#
TXD:MT5351 Transmit
RXD:MT5351 Receiver
TXD1:MT5351& MT8205 Communication
RXD1:MT5351& MT8205 Communication
R1 10K
R2 10K
change 2/16
R354 0/NC
R355 0/NC
R356 0
R357 0
DV33B
SCL0 R3 0
SDA0 R4 0
LRCK R222 0/NC
DATA0 R230 0/NC
R229 0 LRCK
R228 0 DATA0
HDMIMCLK
HDMIBCLK
HDMILRCK
HDMISD0
VI0 VI1 VI2 VI3
U30 74LVC245A
VI4 VI5 VI6 VI7
VI8 VI9 VI10 VI11
U31 74LVC245A
VI12 VI13 VI14 VI15
VI16 VI17 VI18 VI19
U32 74LVC245A
VI20 VI21 VI22 VI23
HDMIHSYNC
HDMIVSYNC
HDMIDE
HDMIODCK
U33 74LVC245A
J24
CCIR_V6
READY#
REQUEST#
CON50
FOR MT5351 INTERFACE
DTV POWER CONTROL
V5V
V9V
CE142 220uF/16v/NC
CB204 0.1uF/NC
CE143 220uF/16v/NC
CB205 0.1uF/NC
U45
IRF7316
SOp8/SMD
VCC
9V
LO = > DTV BOARD POWER OFF
HI = > DTV BOARD POWER ON
R640 22k/NC
R641 22k/NC
R713 22k/NC
R712 22k/NC
R786 0/NC
R787 0/NC
R788 0/NC
Trace width of 12V>30mil
Trace width of 5V >40mil
R642 10k
R643 0/NC
GPIO3
Q31 2N3904 SOT23/SMD/NC
C601 1uF/NC
C602 1uF/NC
J1
7x1 DIP7/P2.0/NC
KAWA Confidential
Title
MT5351 INTERFACE
Size B
Document Number AKAI_MT8202_27US_LVDS_V0.0
<Designer>
Checked: <Checker>
Rev 1
Date: Thursday, April 13, 2006
Sheet 7 17

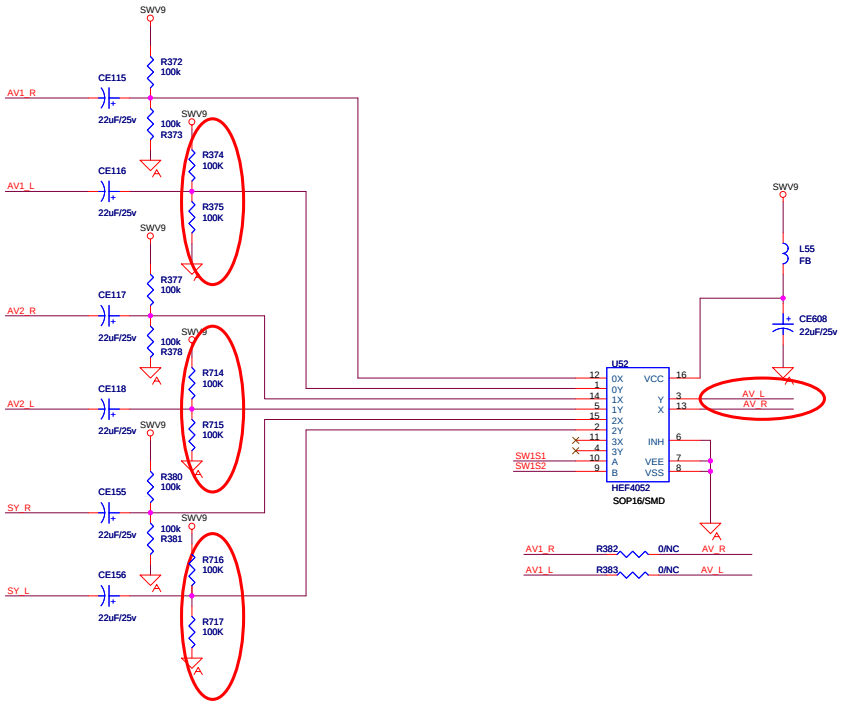
INPUT

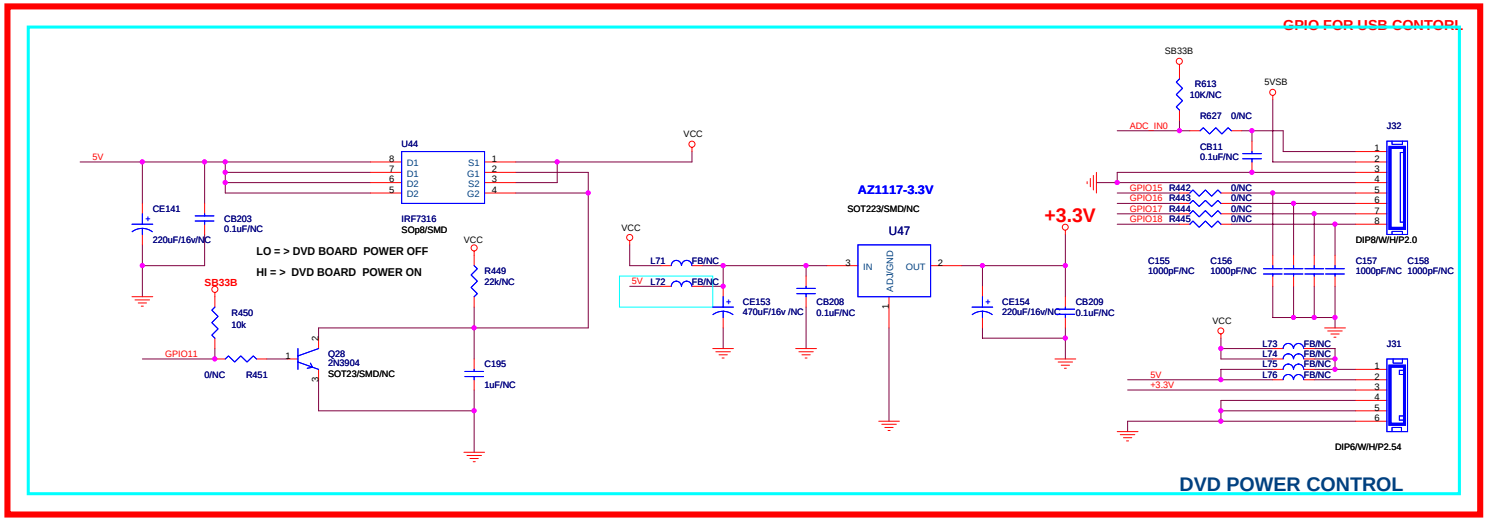
ADC_IN0	ADC_IN0	3
CCIR_V0	CCIR_V0	3
CCIR_V5	CCIR_V5	3
CCIR_V7	CCIR_V7	3
GPIO11	GPIO11	3
GPIO15	GPIO15	3
GPIO16	GPIO16	3
GPIO17	GPIO17	3
GPIO18	GPIO18	3
VFE_GND	VFE_GND	2,3,4,11
AADCVSS	AADCVSS	3,4,10
AV1_R	AV1_R	15
AV1_L	AV1_L	15
AV2_R	AV2_R	15
AV2_L	AV2_L	15
SY_R	SY_R	15
SY_L	SY_L	15
Y2_INB	Y2_INB	15
Y2_GNDB	Y2_GNDB	10,15
CB2_INB	CB2_INB	15
CB2_GNDB	CB2_GNDB	10,15
CR2_INB	CR2_INB	15
CR2_GNDB	CR2_GNDB	10,15
Y3_INB	Y3_INB	15
Y3_GNDB	Y3_GNDB	15
CB3_INB	CB3_INB	15
CB3_GNDB	CB3_GNDB	15
CR3_INB	CR3_INB	15
CR3_GNDB	CR3_GNDB	15
9V	9V	1,7,9,14

OUTPUT

AV_R	AV_R	9
AV_L	AV_L	9
YQ	YQ	10
CBQ	CBQ	10
CRQ	CRQ	10
YQ_GND	YQ_GND	10
CBQ_GND	CBQ_GND	10
CRQ_GND	CRQ_GND	10







KAWA Confidential

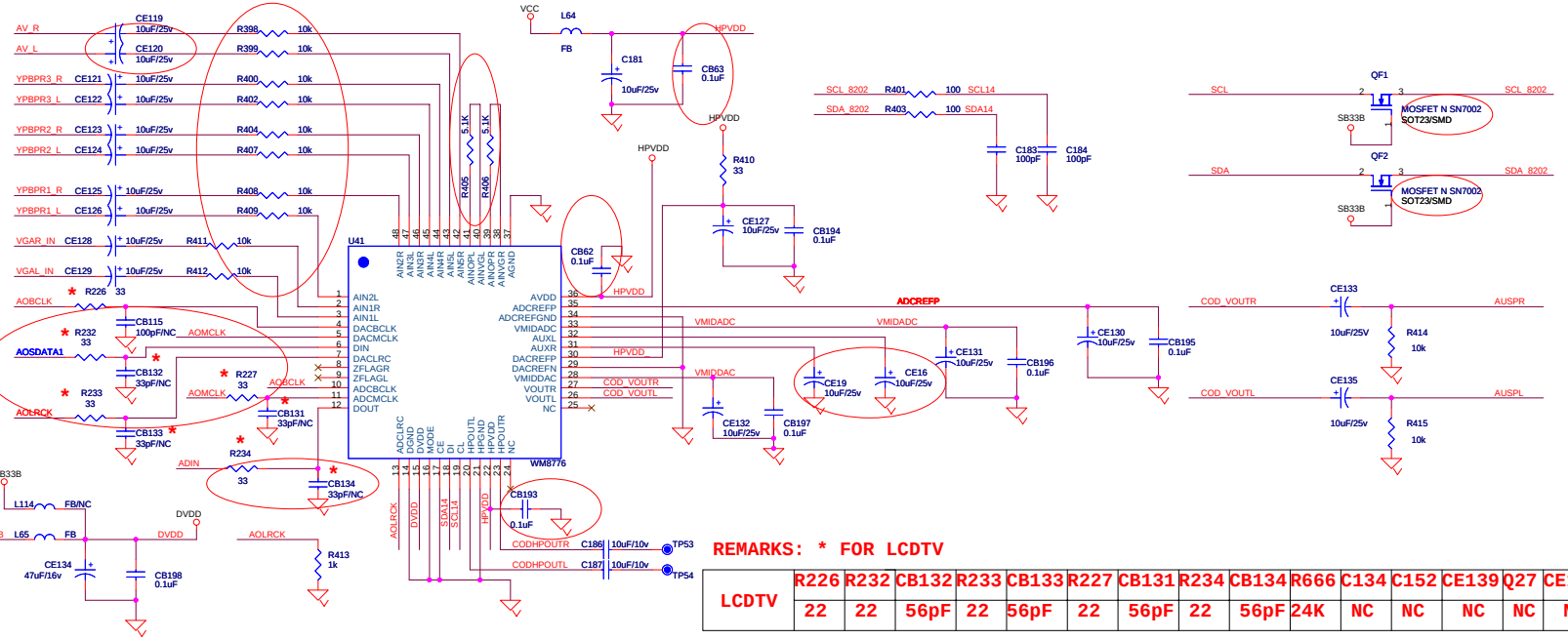
Title: DAUGHTER BOARD IN			
Size: C	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, April 13, 2006		Sheet 8	17

INPUT

GPIO7	GPIO7	3
SCL	SCL	1,14
SDA	SDA	1,14
SDA_8202	SDA_8202	3,6,12
SCL_8202	SCL_8202	3,6,12
AOSDATA1	AOSDATA1	3
AOMCLK	AOMCLK	3,16
AOBCLK	AOBCLK	3,16
AOLRCK	AOLRCK	3,16
ADIN	ADIN	3
AV_R	AV_R	8
AV_L	AV_L	8
YPBPR1_L	YPBPR1_L	15
YPBPR1_R	YPBPR1_R	15
YPBPR2_R	YPBPR2_R	15
YPBPR2_L	YPBPR2_L	15
YPBPR3_R	YPBPR3_R	15
YPBPR3_L	YPBPR3_L	15
VGAR_IN	VGAR_IN	11
VGAL_IN	VGAL_IN	11
TESTP2	TESTP2	3
AR	AR	3
AL	AL	3
MU	MU	16
A_MUTE	A_MUTE	17
9V	9V	1,7,14

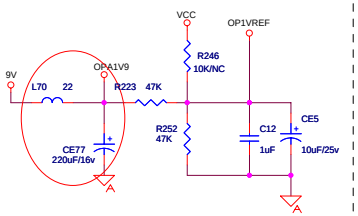
OUTPUT

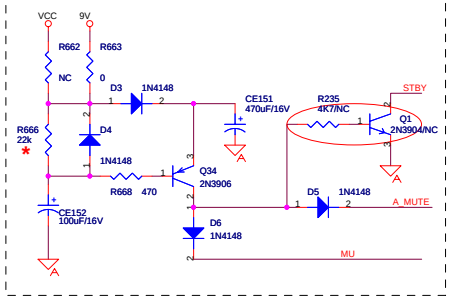
AUSPR	AUSPR	16
AUSPL	AUSPL	16
AVR_OUT	AVR_OUT	15
AVL_OUT	AVL_OUT	15
CVBS_OUT	CVBS_OUT	6,15

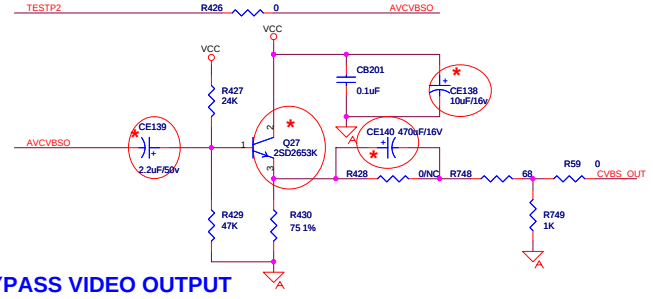


REMARKS: * FOR LCDTV

	R226	R232	CB132	R233	CB133	R227	CB131	R234	CB134	R666	C134	C152	CE139	Q27	CE140	CE138
LCDTV	22	22	56pF	22	56pF	22	56pF	22	56pF	24K	NC	NC	NC	NC	NC	NC

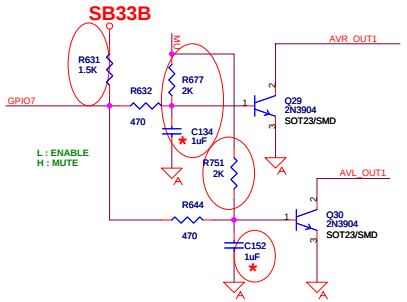




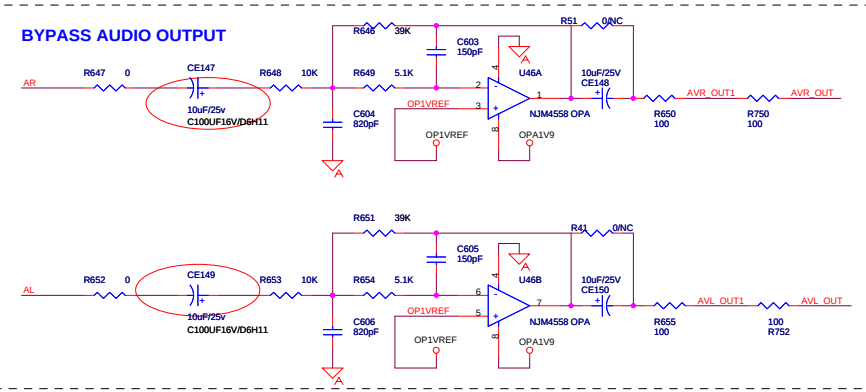


BYPASS VIDEO OUTPUT

AUDIO BYPASS MUTE



BYPASS AUDIO OUTPUT



KAWA Confidential

Title	M8776 & VIDEO BYPASS		
Size C	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
Date: Saturday, April 22, 2006		Sheet 9	17

CVBS0 CVBS1 CVBS2

SY0 SC0

SY1 SC1

Y0+ Y0- PB0+ PB0- PR0+ PR0- SOY0

Y1+ Y1- PB1+ PB1- PR1+ PR1- SOY1

MPX1

MPX2

TO MT8202

TV_GND CVBS_0 SIF AF CVBS_1 CVBS1_GND CVBS_2 CVBS2_GND SY_1 SY_1_GND SC_1 SC_1_GND SY_0 SY_0_GND SC_0 SC_0_GND

SOY1 SOY0 Y1_INB Y1_GNDB CR1_INB CR1_GNDB CB1_INB CB1_GNDB CBQ CRQ YQ YQ_GND CBQ_GND CRQ_GND

FROM AV BOARD

AADCVSS

THIS PAGE NEARLY IC

CVBS_0 R197 0 C110 47nF CVBS0
C113 330pF TV_GND

CVBS_1 R200 0 C117 47nF CVBS1
C120 330pF CVBS1_GND

CVBS_2 R424 0 C188 47nF CVBS2
C189 330pF CVBS2_GND

SY_0 R198 0 C111 47nF SY0
C114 330pF SY_0_GND

SC_0 R201 0 C118 47nF SC0
C121 330pF SC_0_GND

SY_1 R205 0 C125 47nF SY1
C128 330pF SY_1_GND

SC_1 R209 0 C132 47nF SC1
C135 330pF SC_1_GND

R55 0 C112 4.7nF SOY0

YQ R199 68 C115 100nF Y0+
C116 15pF
YQ_GND R202 100 C119 100nF Y0-

CBQ R203 68 C122 100nF PB0+
C123 15pF
CBQ_GND R206 100 C126 100nF PB0-

CRQ R207 68 C129 100nF PR0+
C130 15pF
CRQ_GND R210 100 C133 100nF PR0-

R56 0 C136 4.7nF SOY1

Y1_INB R211 68 C137 100nF Y1+
C138 15pF
Y1_GNDB R213 100 C140 100nF Y1-

CB1_INB R214 68 C141 100nF PB1+
C142 15pF
CB1_GNDB R217 100 C145 100nF PB1-

CR1_INB R218 68 C146 100nF PR1+
C147 15pF
CR1_GNDB R219 100 C148 100nF PR1-

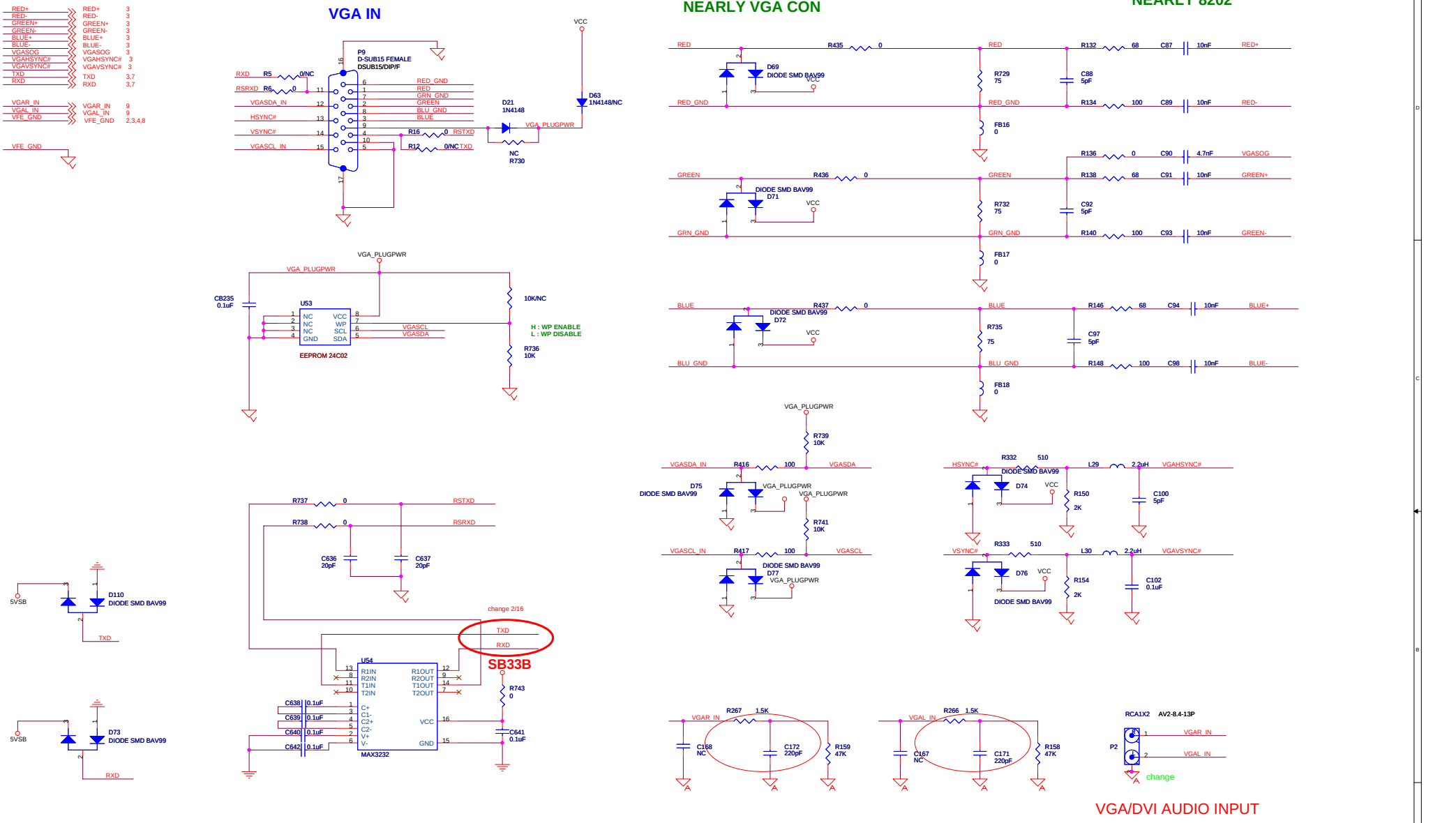
FROM Tuner

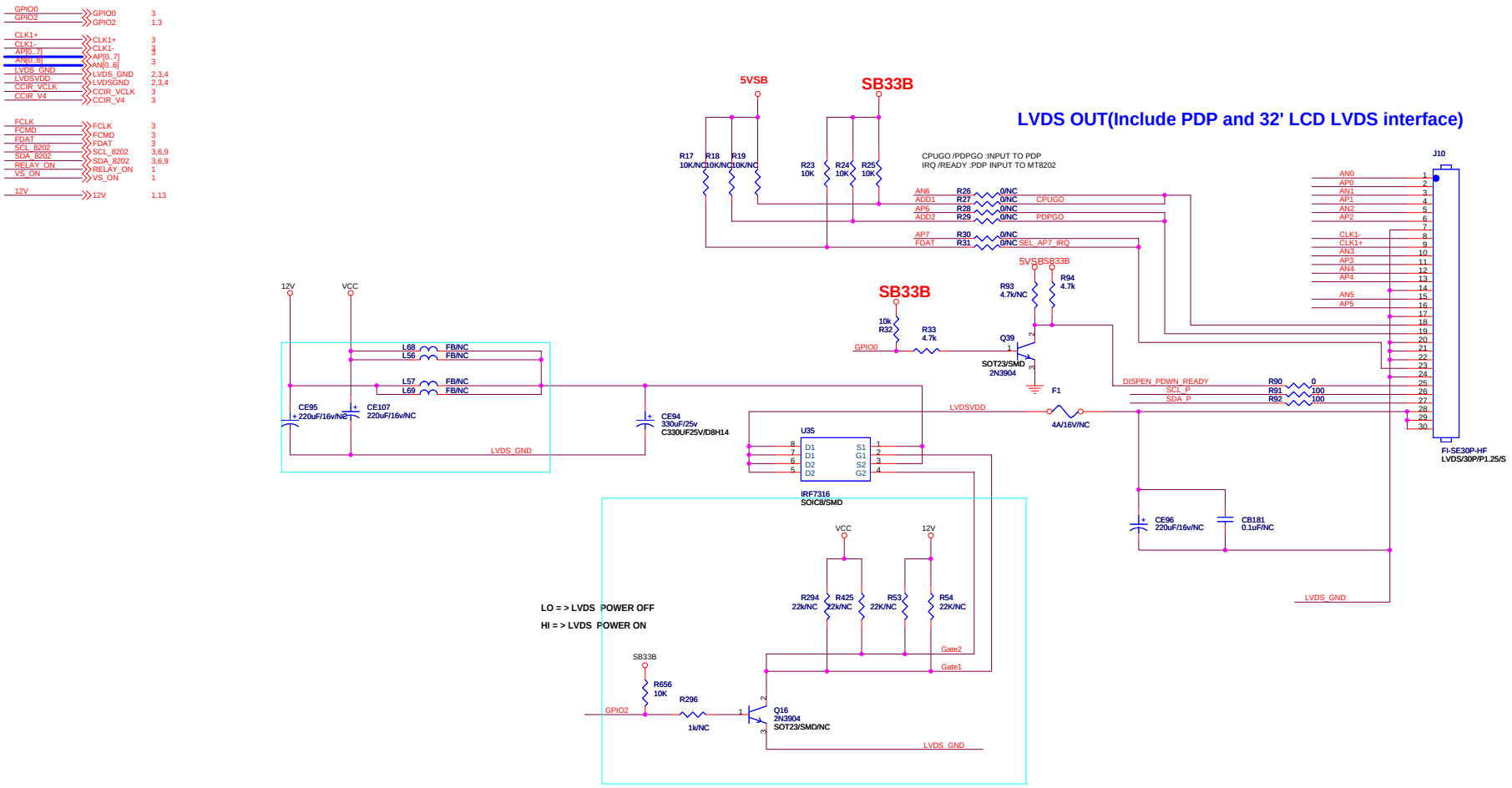
SIF R212 8.2K C139 10nF MPX1
C48 1.8pF AADCVSS

AF R215 39K R216 39K CE70 + 47uF/16V MPX2
C143 15pF C144 15pF AADCVSS

KAWA Confidential

Title	AUDIO / VIDEO IN CIRCUIT		
Size C	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
Date: Thursday, April 13, 2006		Sheet 10 17	

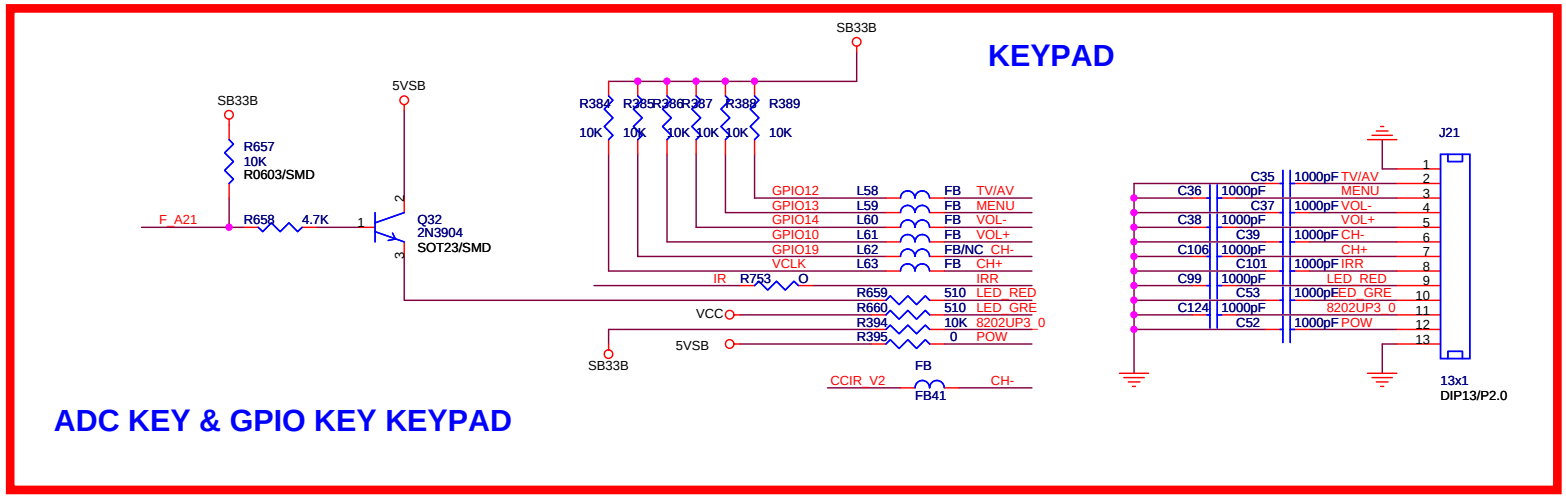

VGA IN
NEARLY VGA CON
NEARLY 8202
RED+ RED- GREEN+ GREEN- BLUE+ BLUE- VGASOG VGAHSYNC# VGAVSYNC# TXD RXD
VGAR_IN VGAL_IN VFE_GND
P9 D-SUB15 FEMALE DSUB15/DIP/F
RED_GND RED GRN_GND GREEN BLU_GND BLUE
VGASDA_IN HSYNC# VSYNC# VGASCL_IN
R5 0/NC R6 0 R16 0 RSTXD R12 0/NC TXD
D21 1N4148 NC R730 VGA_PLUGPWR
D63 1N4148/NC VCC
D69 DIODE SMD BAV99
R435 0 R729 75 R132 68 C87 10nF C88 5pF R134 100 C89 10nF FB16 0
D71 DIODE SMD BAV99
R436 0 R732 75 R136 0 C90 4.7nF R138 68 C91 10nF C92 5pF R140 100 C93 10nF FB17 0
D72 DIODE SMD BAV99
R437 0 R735 75 R146 68 C94 10nF C97 5pF R148 100 C98 10nF FB18 0
CB235 0.1uF
U53 NC NC NC GND VCC WP SCL SDA
EEPROM 24C02
10K/NC R736 10K
H : WP ENABLE
L : WP DISABLE
R739 10K
D75 DIODE SMD BAV99
R416 100 R741 10K
D77 DIODE SMD BAV99
R417 100
R737 0 R738 0
C636 20pF C637 20pF
change 2/16
SB33B
U54 MAX3232
R743 0
C638 C639 C640 C642 0.1uF
C641 0.1uF
D110 DIODE SMD BAV99
D73 DIODE SMD BAV99
5VSB
R332 510 L29 2.2uH R150 2K C100 5pF
D74 DIODE SMD BAV99
R333 510 L30 2.2uH R154 2K C102 0.1uF
D76 DIODE SMD BAV99
R267 1.5K C168 NC C172 220pF R159 47K
R266 1.5K C167 NC C171 220pF R158 47K
RCA1X2 AV2-8.4-13P
P2
change
VGA/DVI AUDIO INPUT
KAWA Confidential
VGA IN & PC AUDIO IN
Document Number AKAI_MT8202_27US_LVDS_V0.0
Rev 1
Thursday, April 13, 2006
Sheet 11 17

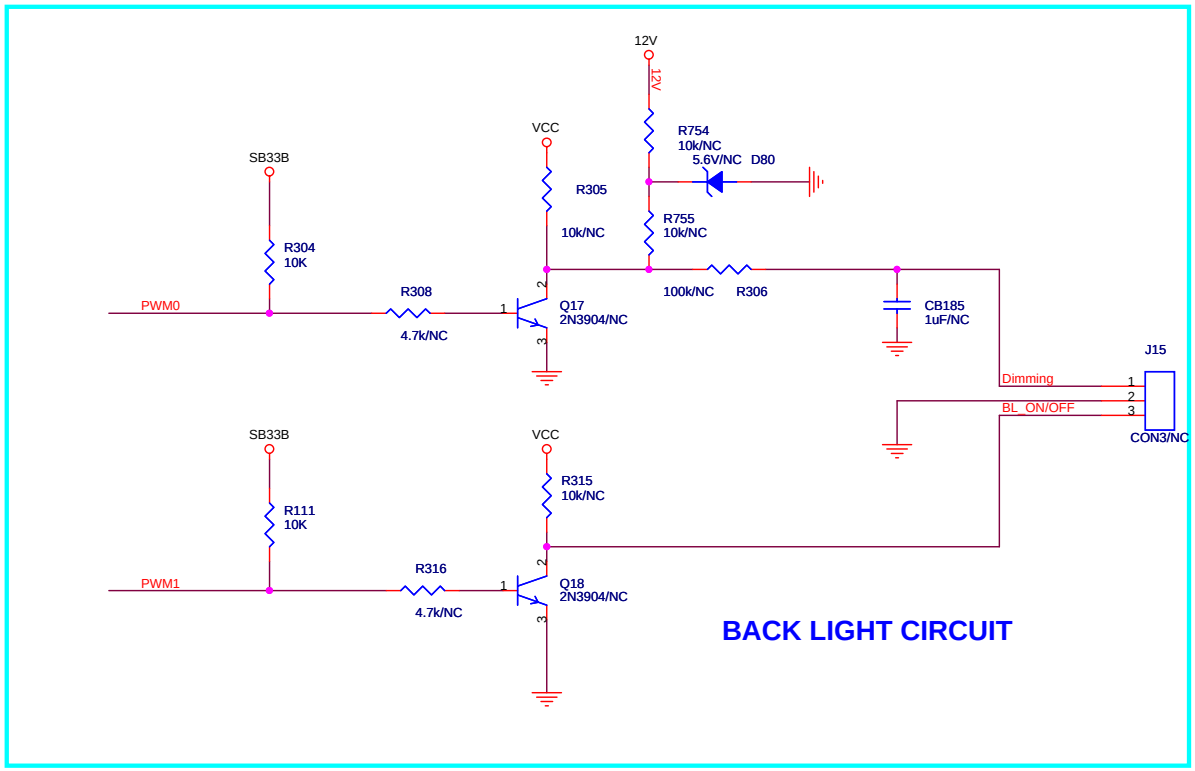


KAWA Confidential

Title	LVDS OUT		
Size C	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
Date: Thursday, April 13, 2006		Sheet 12	17

IR	IR	3,15
GPIO10	GPIO10	3
GPIO12	GPIO12	3
GPIO13	GPIO13	3
GPIO14	GPIO14	1,3
PWM0	PWM0	3
PWM1	PWM1	3
8202UP3_0	8202UP3_0	3
GPIO14	GPIO14	1,3
GPIO19	GPIO19	1,3
VCLK	VCLK	3
F_A21	F_A21	3
CCIR_V2	CCIR_V2	3
12V	12V	1,12





KAWA Confidential

Title: BACK LIGHT / KEYPAD			
Size: B	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, April 13, 2006		Sheet 13	17

SCL
SDA
CVBS_0
TV_GND
AF
SIF
ADC_IN4
9V

SCL 1,9
SDA 1,9
CVBS_0 10
TV_GND 10
AF 10
SIF 10
ADC_IN4 3
9V 1,7,9

TUNER SIF1NTSC 4.5MHz BPF

SIF_9V
CE617 10uF/25v C10UF25V/D4H5
R423 1K
R422 1.8K
C645 10nF
SIF
SIF1_IN
C646 10nF
R418 0
1000pF/27pF C647
FB19 3.3uH/22uH
BEAD/SMD/1210
C648 10nF
Q40 2N3904 SOT23/SMD
C649 820pF 560pF
L87 1.5uH 1.2uH
C650 820pF 560pF
L88 1.5uH 1.2uH
2.2uH
R419 220
R420 10
R421 71.5
C651 NC

FQ1216 : PAL
FQ1236 : NTSC

ADDRESS
TUNER IF
C0 84

TU1
FQ1236-MK3
GND1 GND2 NC BT VS_TUNER SCL SDA AS AFC NC NC NC 2nd SIF OUT CVBS VS_IF AF/MPX GND3 GND4
21 22 1 2 3 4 5 6 7 8 9 10 11 12 13 14 23 24
VS_TUNER
VS_IF
SCL R231 100
SDA R208 100
TU_AV
C675 20pF
C676 20pF
AFC
SIF1_IN
AF1_IN

AF1_IN CE626 33uF/16V AF
VCC
R178 R/NC
ADC_IN4 R180 0/NC AFC
R179 R/NC
C191 20pF

U59
ADD
9V
CE635 220uF/10V
CB247 0.1uF
IN ADJ/GND OUT
TO220/DIP
7805
加散热片，尺寸与atsc Board 相同
TU_VCC
CE618 220uF/10V
L89 470uH
L/IND/SMD/SLF7032
VS_TUNER
FB12 BEAD/SMD/1206 NC
CE620 470uF/16V
CB236 0.1uF

TU_VCC
L91 470uH
L/IND/SMD/SLF7032
VS_IF
FB14 BEAD/SMD/1206 NC
CE625 470uF/16V
CB239 0.1uF

9V
FB21 47
SWV9
CE629 47uF/16V
CE630 220uF/16V
CB242 0.1uF
FB22 FB
SIF_9V
CE634
CB243 0.1uF

TU_AV
L93 2.2uH
L/IND/SMD/0805
TU_CVBS
R317 18
R58 0 CVBS_0
C656 330pF
C657 330pF
R318 56
TV_GND
FB20 0

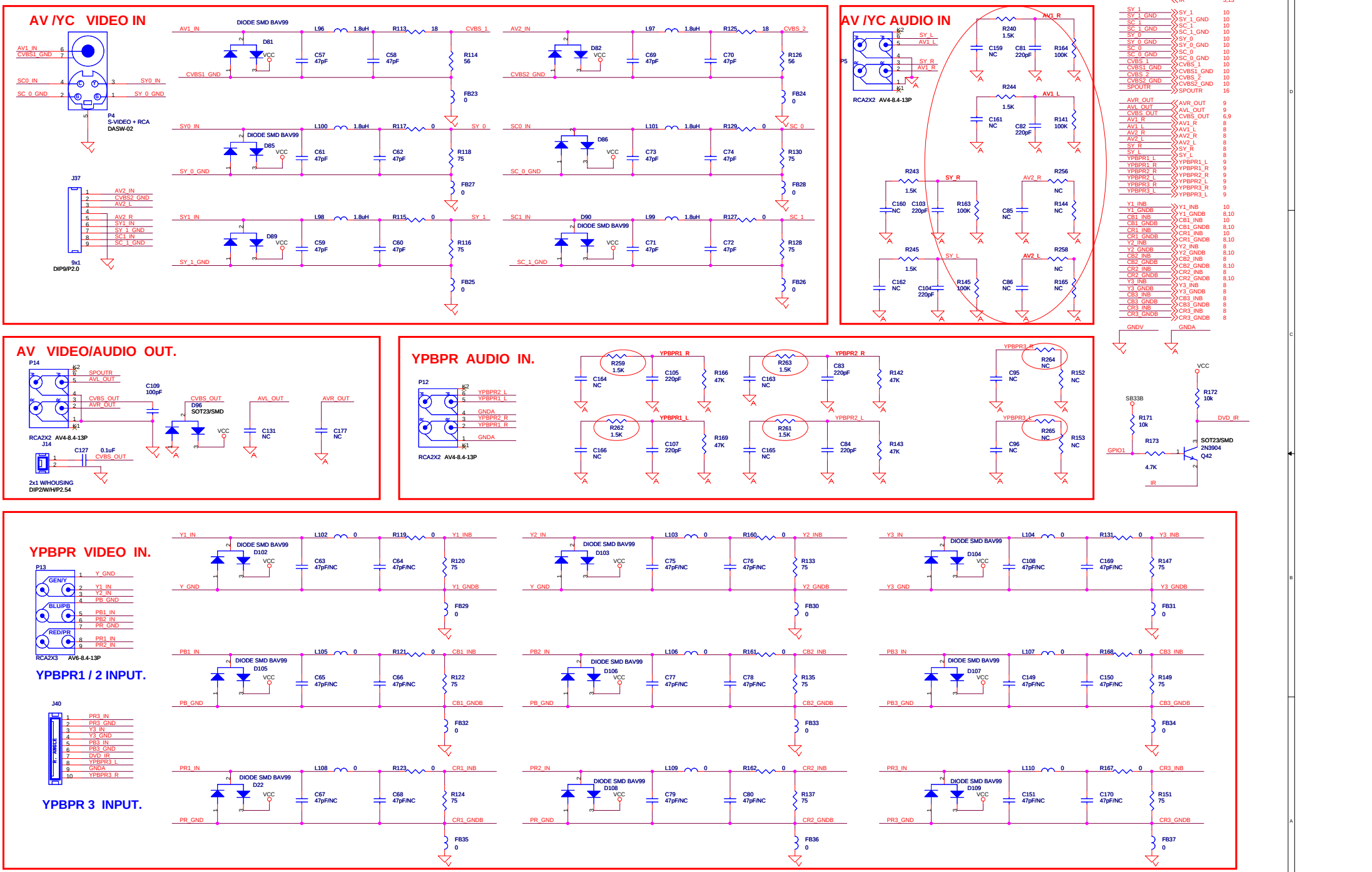
J9
TU_VCC 1
TU_AV 2
TV_GND 3
SIF1_IN 4
AF1_IN 5
6
7
SCL 8
SDA 9
AFC 10
11
DIP11/W/H/P2.0

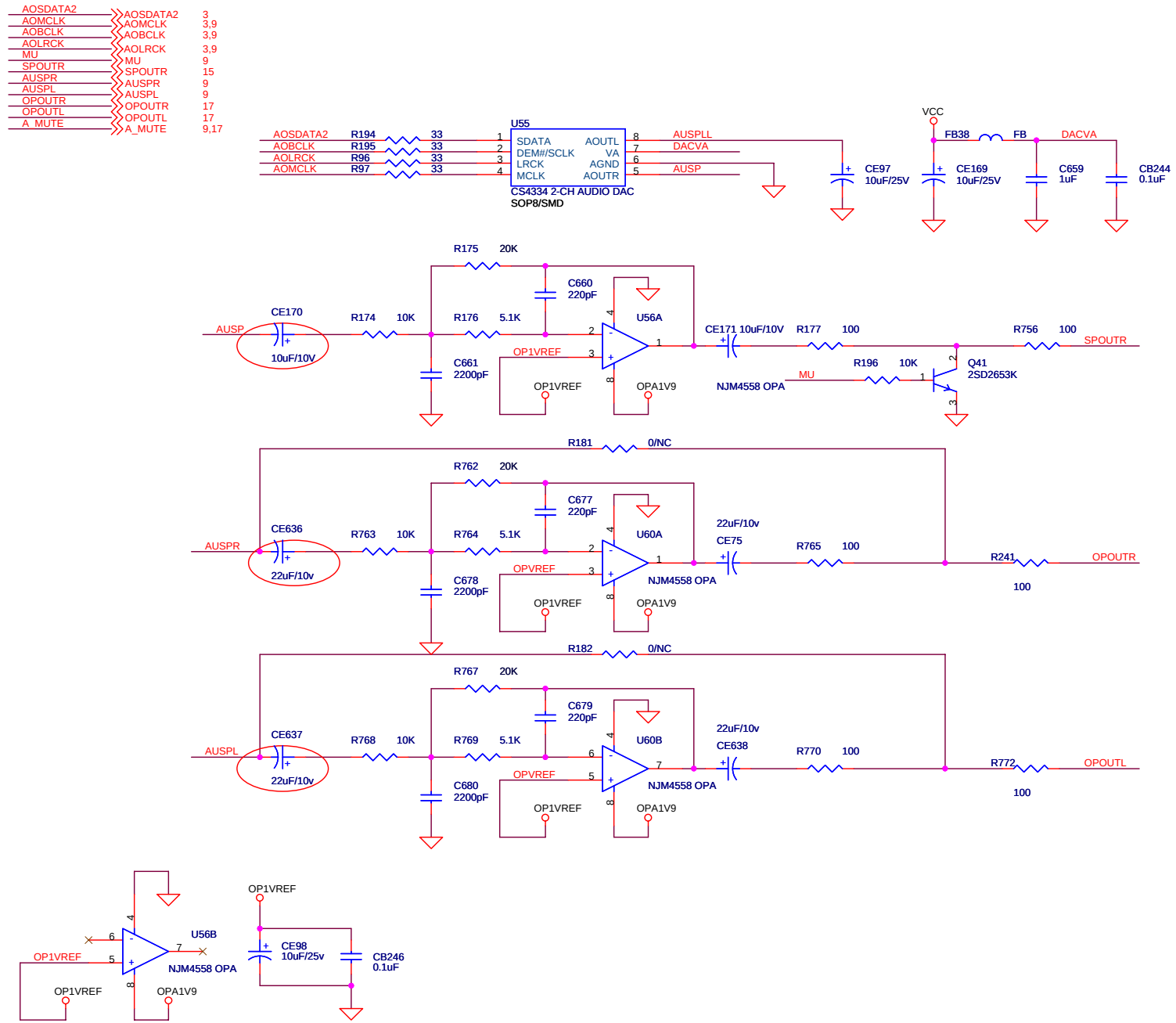
J16
SIF 1
AF 2
3
4
CVBS_0 5
TV_GND 6
SCL 7
SDA 8
8x1
DIP8/P2.0

KAWA Confidential

Title	<Title>		
Size Custom	Document Number <Doc>		Rev <RevCode>
Date: Thursday, April 13, 2006	Sheet 1 of 1		

Title	TUNER IN		
Size Custom	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
Date: Thursday, April 13, 2006	Sheet 14		17


AV /YC VIDEO IN
AV1_IN
CVBS1_GND
SC0_IN
SC_0_GND
SY0_IN
SY_0_GND
P4
S-VIDEO + RCA
DASW-02
J37
AV2_IN
CVBS2_GND
AV2_L
AV2_R
SY1_IN
SY_1_GND
SC1_IN
SC_1_GND
9x1
DIP9/P2.0
DIODE SMD BAV99
L96 1.8uH
R113 18
CVBS_1
D81
C57 47pF
C58 47pF
R114 56
FB23 0
L97 1.8uH
R125 18
CVBS_2
D82
C69 47pF
C70 47pF
R126 56
FB24 0
L100 1.8uH
R117 0
SY_0
D85
C61 47pF
C62 47pF
R118 75
FB27 0
L101 1.8uH
R129 0
SC_0
D86
C73 47pF
C74 47pF
R130 75
FB28 0
L98 1.8uH
R115 0
SY_1
D89
C59 47pF
C60 47pF
R116 75
FB25 0
L99 1.8uH
R127 0
SC_1
D90
C71 47pF
C72 47pF
R128 75
FB26 0
VCC
AV /YC AUDIO IN
P5
RCA2X2 AV4-8.4-13P
SY_L
AV1_L
SY_R
AV1_R
R240 1.5K
C159 NC
C81 220pF
R164 100K
R244 1.5K
C161 NC
C82 220pF
R141 100K
R243 1.5K
C160 NC
C103 220pF
R163 100K
C85 NC
R144 NC
R256 NC
R245 1.5K
C162 NC
C104 220pF
R145 100K
C86 NC
R165 NC
R258 NC
AV /VIDEO/AUDIO OUT.
P14
RCA2X2 AV4-8.4-13P
J14
2x1 W/HOUSING
DIP2/W/H/P2.54
SPOUTR
AVL_OUT
CVBS_OUT
AVR_OUT
C109 100pF
D96 SOT23/SMD
C127 0.1uF
C131 NC
C177 NC
YPBPR AUDIO IN.
P12
RCA2X2 AV4-8.4-13P
YPBPR2_L
YPBPR1_L
GNDA
YPBPR2_R
YPBPR1_R
R259 1.5K
C164 NC
C105 220pF
R166 47K
R262 1.5K
C166 NC
C107 220pF
R169 47K
R263 1.5K
C163 NC
C83 220pF
R142 47K
R261 1.5K
C165 NC
C84 220pF
R143 47K
YPBPR3_R
YPBPR3_L
R264 NC
C95 NC
R152 NC
R265 NC
C96 NC
R153 NC
GNDV
GNDA
VCC
R172 10k
SB33B
R171 10k
DVD_IR
GPIO1
R173
SOT23/SMD
2N3904
Q42
4.7K
IR
YPBPR VIDEO IN.
P13
RCA2X3 AV6-8.4-13P
GEN/Y
BLU/PB
RED/PR
Y_GND
Y1_IN
Y2_IN
PB_GND
PB1_IN
PB2_IN
PR_GND
PR1_IN
PR2_IN
YPBPR1 / 2 INPUT.
J40
PR3_IN
PR3_GND
Y3_IN
Y3_GND
PB3_IN
PB3_GND
DVD_IR
YPBPR3_L
GNDA
YPBPR3_R
YPBPR 3 INPUT.
L102 0
R119 0
Y1_INB
D102
C63 47pF/NC
C64 47pF/NC
R120 75
Y1_GNDB
FB29 0
L103 0
R160 0
Y2_INB
D103
C75 47pF/NC
C76 47pF/NC
R133 75
Y2_GNDB
FB30 0
L104 0
R131 0
Y3_INB
D104
C108 47pF/NC
C169 47pF/NC
R147 75
Y3_GNDB
FB31 0
L105 0
R121 0
CB1_INB
D105
C65 47pF/NC
C66 47pF/NC
R122 75
CB1_GNDB
FB32 0
L106 0
R161 0
CB2_INB
D106
C77 47pF/NC
C78 47pF/NC
R135 75
CB2_GNDB
FB33 0
L107 0
R168 0
CB3_INB
D107
C149 47pF/NC
C150 47pF/NC
R149 75
CB3_GNDB
FB34 0
L108 0
R123 0
CR1_INB
D22
C67 47pF/NC
C68 47pF/NC
R124 75
CR1_GNDB
FB35 0
L109 0
R162 0
CR2_INB
D108
C79 47pF/NC
C80 47pF/NC
R137 75
CR2_GNDB
FB36 0
L110 0
R167 0
CR3_INB
D109
C151 47pF/NC
C170 47pF/NC
R151 75
CR3_GNDB
FB37 0
KAWA Confidential
Title
AV IN
Size C
Document Number AKAI_MT8202_27US_LVDS_V0.0
Rev 1
<Designer>
Checked: <Checker>
Date: Thursday, April 13, 2006
Sheet 15 17

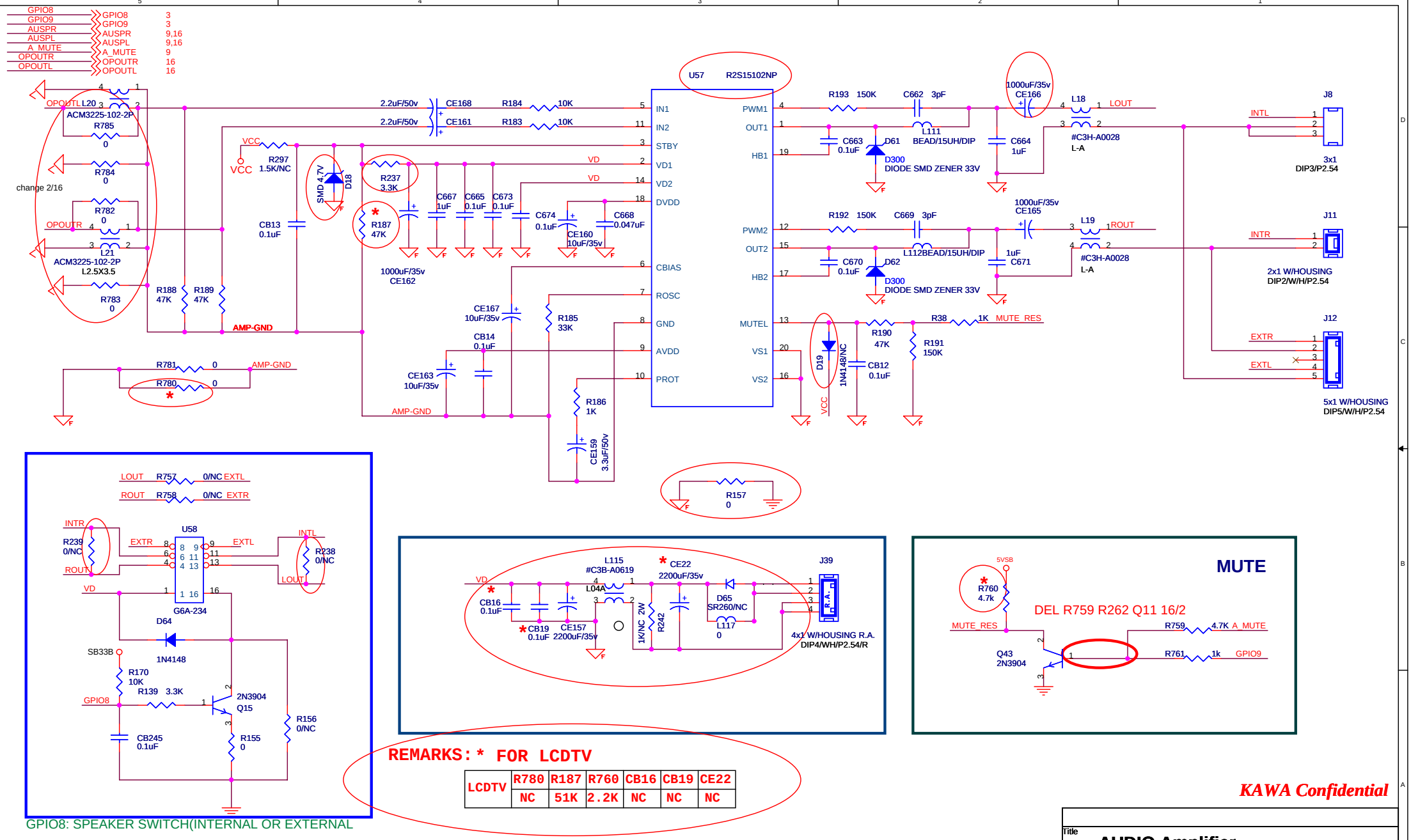


GPIO DECRIPTION

UP3_4 : SW SCL
UP3_5 : SW SDA
ERO0/UP3_0 :KEYPAD POWER
ERO1/UP3_1 : MAIN POWER SWITCH
VCLK : KEPAD CH+
GPIO19 : KEPAD CH-
DE/GPIO : DVD IR
CCIR_CLK : PDP USE
CCIR_V4 : PDP USE
GPIO0 : PDP USE
GPIO1 : NO USE
GPIO2 : LVDS POWER SW
GPIO3 : DTV POWER CONTROL
GPIO4 : EEPROM WRITE PROTECT
GPIO5/TXD : 2nd UART FOR MT5351
GPIO6/RXD : 2nd UART FOR MT5351
GPIO7 : AUDIO BYPASS MUTE CONTROL
GPIO8 : SPEAKER SWITCH
GPIO9 : AUDIO MUTE
GPIO10 : Indicates active video at HDMI port
GPIO11 : DVD POWER CONTROL
GPIO12 : AV SWITCH
GPIO13 : HDMI Hot Plug Detect
GPIO14 : NO USE
GPIO[15..18] : FOR DVD CONTROL
GPIO/PWM0 : DIMMING
GPIO/PWM1 : BACKLIGHT ON/OFF
OUT_27Mhz/GPIO : HDMI CRYSTAL
SDA1 : TO MT5351 I/F REQUEST
SCL1 : TO MT5351 I/F READY
F_A21 : KEYPAD(LED RED)
ADCIN0 : KEYPAD
ADCIN3:PDP 5VD DETECT
ADCIN4:FOR TUNER AFC

CCIR_V[0-3] : KEYPAD
CCIR_V5 : AUDIO SWITCH
CCIR_V6 : RESET DTV
CCIR_V7 : YPBPR VIDEO SWITCH

Title: SUB WOOFER			
Size: B	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, April 13, 2006		Sheet 16	17



GPIO8: SPEAKER SWITCH(INTERNAL OR EXTERNAL

REMARKS: * FOR LCDTV

LCDTV	R780	R187	R760	CB16	CB19	CE22
	NC	51K	2.2K	NC	NC	NC

KAWA Confidential

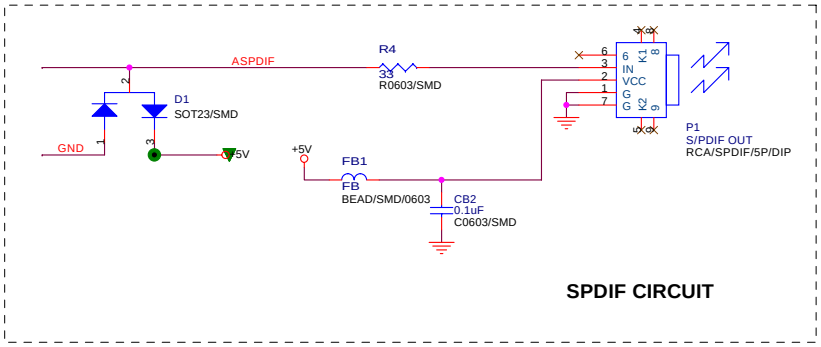
Title: AUDIO Amplifier			
Size: B	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
Date: Saturday, April 22, 2006		Sheet 17	17

MT5111 / MT5351 REFERENCE DESIGN - 4 LAYERS

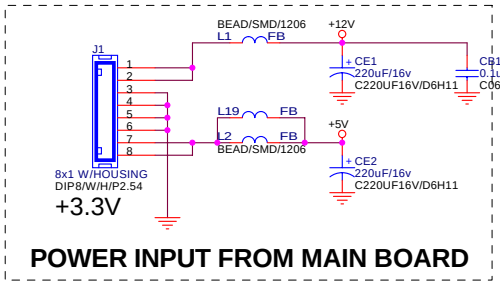
Rev	History	P#	DATE
RA-V1	INITIAL VERSION		2005/06/15
RA-V2	ADDED AUDIO SWITCH / REFINE POWER CIRCUIT		2005/07/14

NS : NON-STUFF

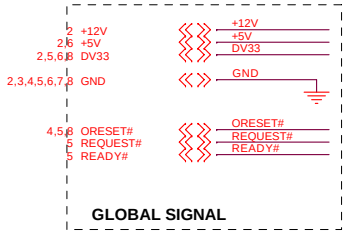
NAME	TYPE	DEVICE
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5V_tuner	POWER +5V	TUNER POWER
DV33_DM	POWER +3V3	MT5111 POWER
DV18	POWER +1V8	MT5111 POWER
DV33	POWER +3V3	MT5351 POWER
AV33	POWER +3V3	MT5351 ANALOG POWER
DV25	POWER +2V5	MT5351 DDR POWER
DV12	POWER +1V2	MT5351 POWER
GND	GROUND	GROUND



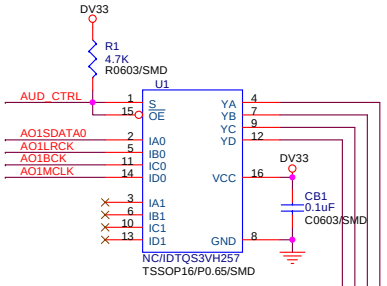
SPDIF CIRCUIT

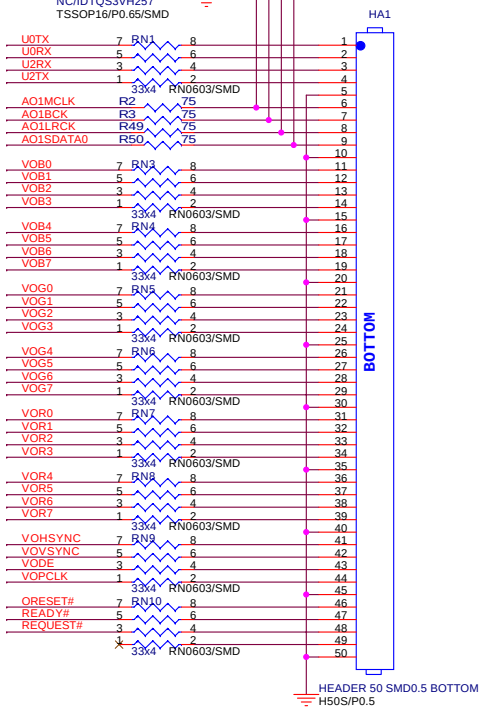


POWER INPUT FROM MAIN BOARD

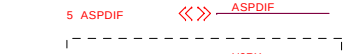


GLOBAL SIGNAL

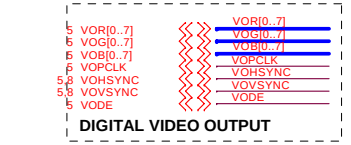




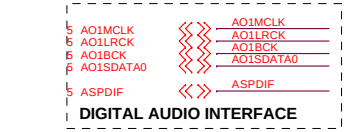
DIGITAL OUTPUT



UART (RS232)



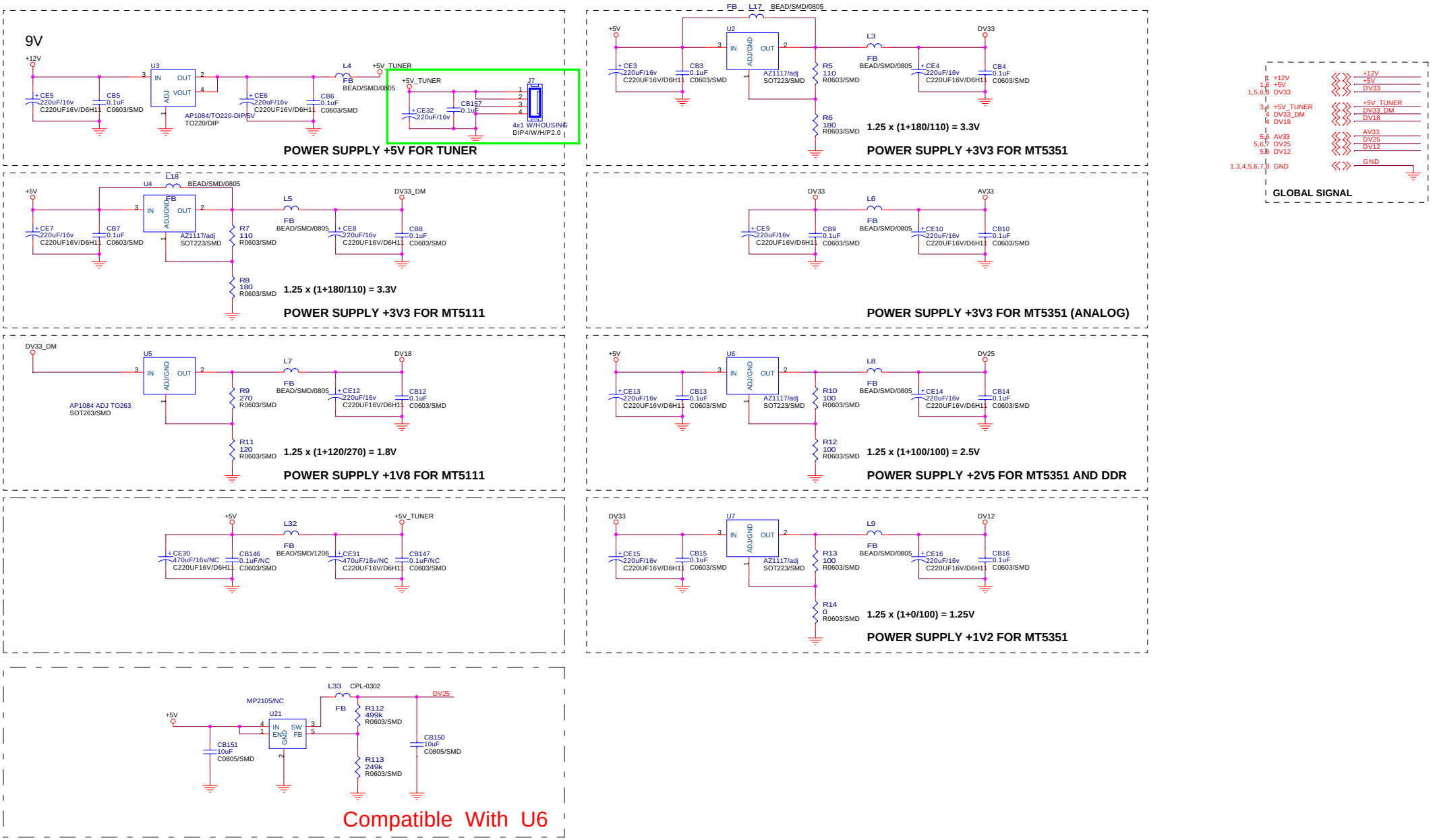
DIGITAL VIDEO OUTPUT



DIGITAL AUDIO INTERFACE

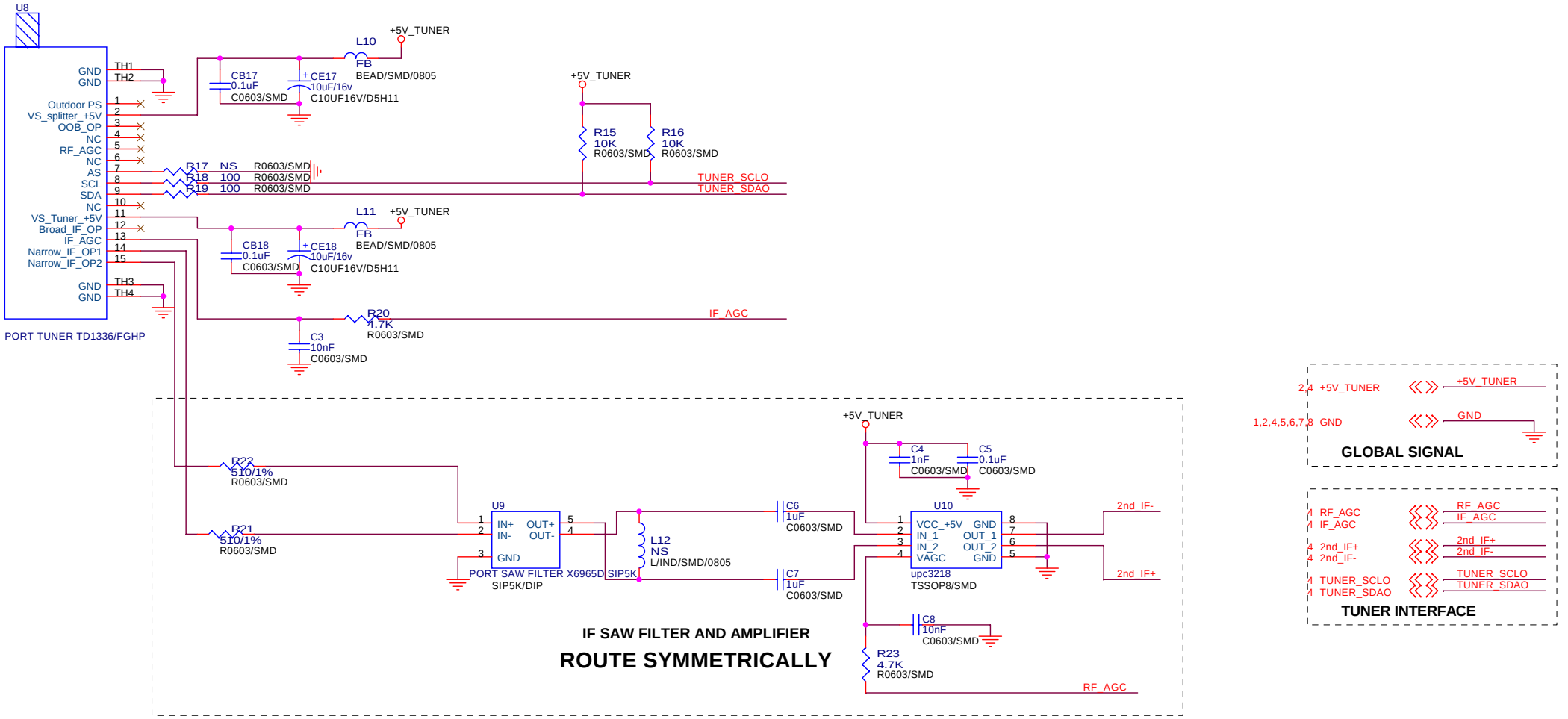
MediaTek Confidential

Title: INDEX		
Size: Custom	Document Number: MT5351RA-V2	Rev: 1
Date: Monday, February 20, 2006	TwinSon Chan	Sheet 1 of 8



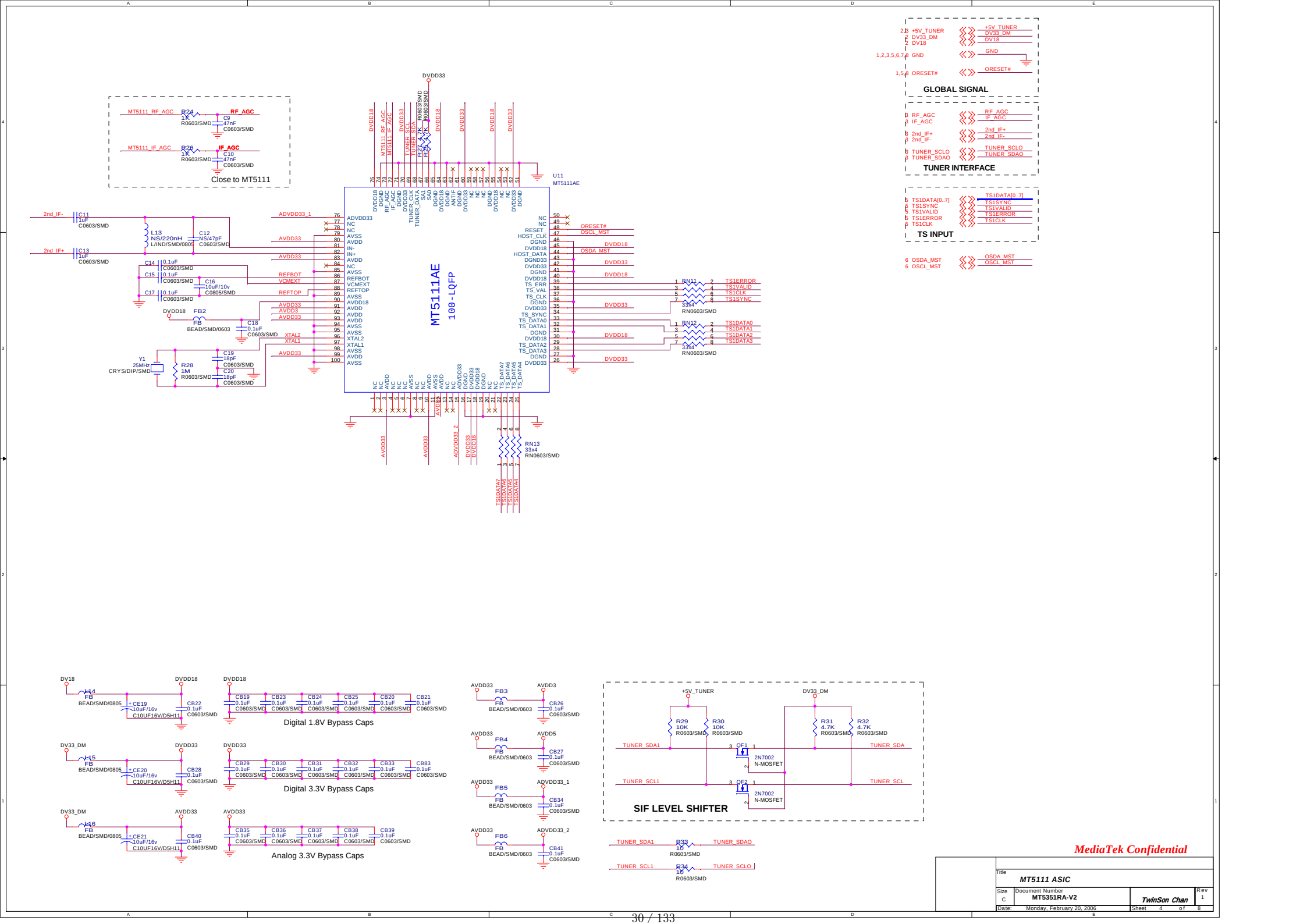
MediaTek Confidential

Title: POWER		
Size: Custom	Document Number: MT5351RA-V2	Rev: 1
Date: Monday, February 20, 2006	Sheet 2 of 8	TwinSon Chan



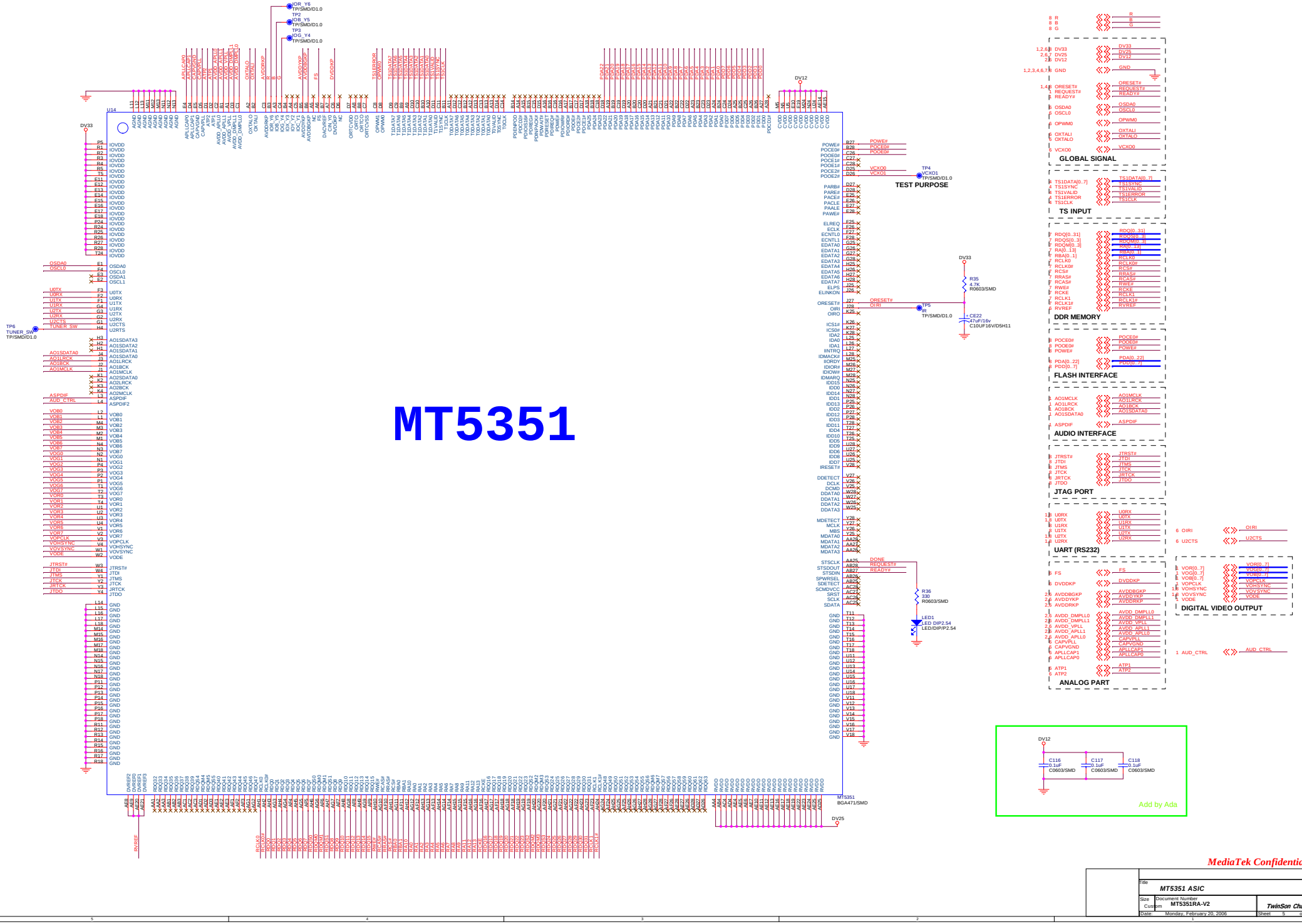
MediaTek Confidential

Title: TUNER			
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006		Sheet 3 of 8	

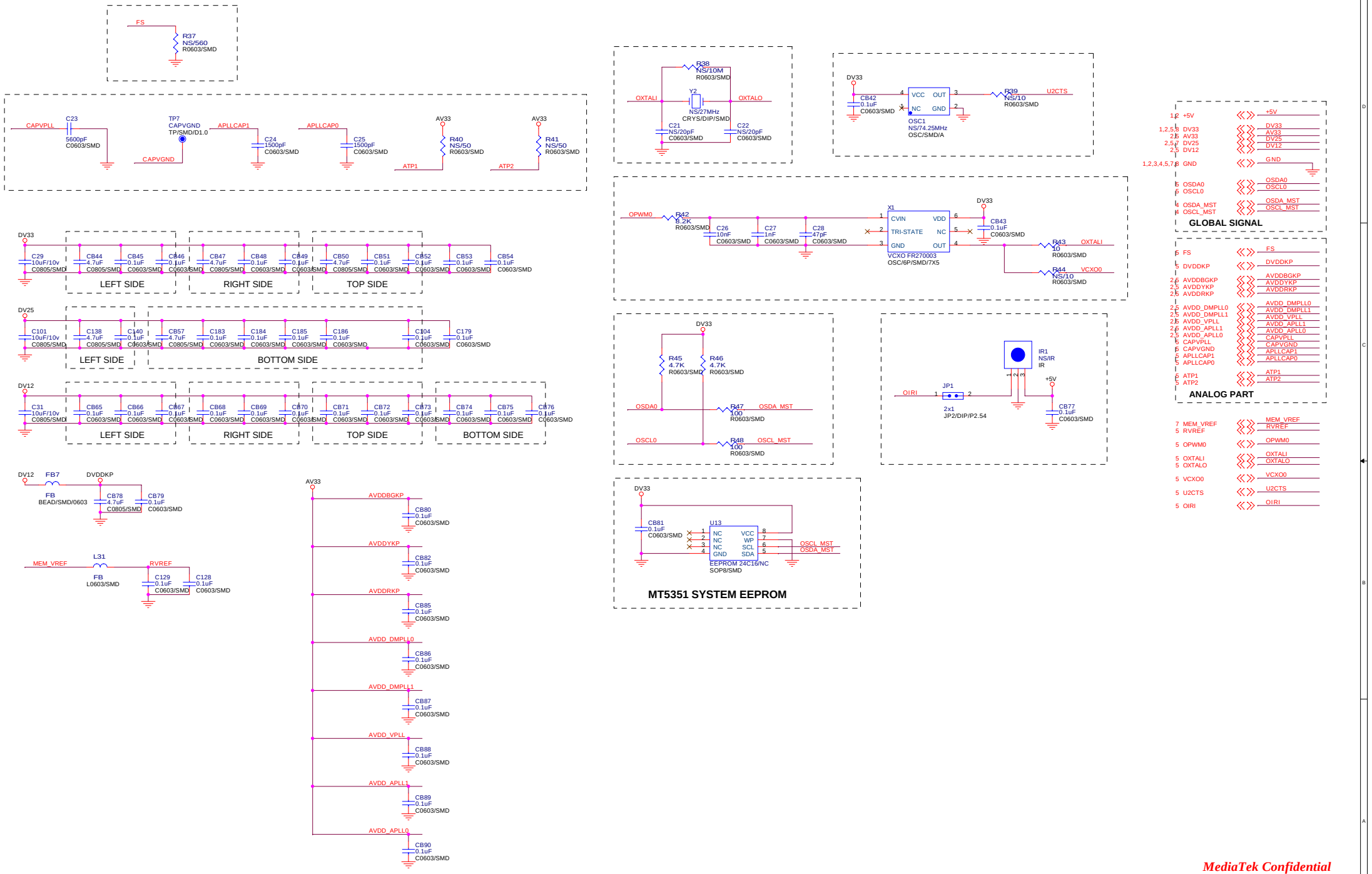


MediaTek Confidential

Title: MT5111 ASIC			
Size: C	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006		Sheet 4 of 8	

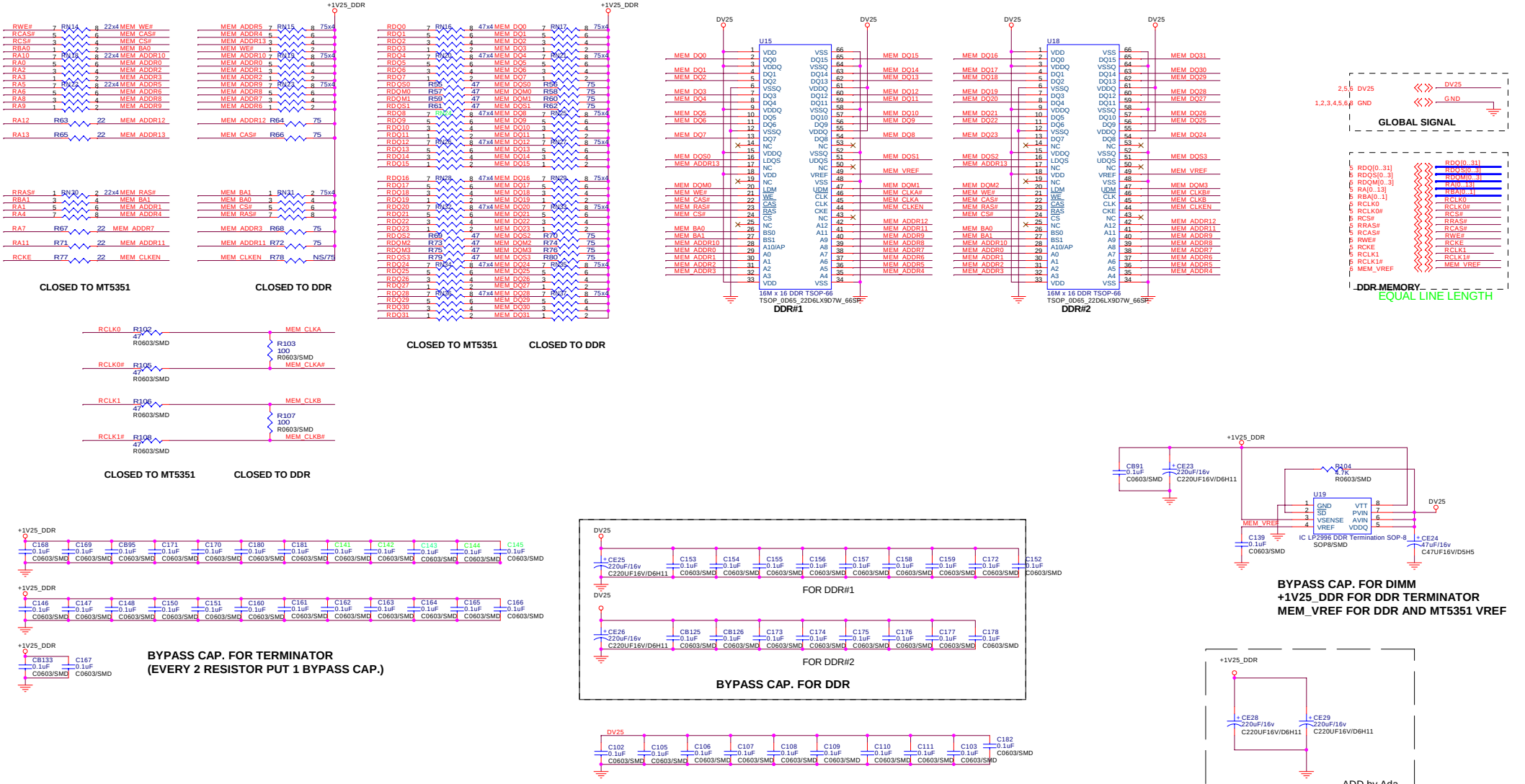


Title	MT5351 ASIC		
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006	Sheet 5 of 8		

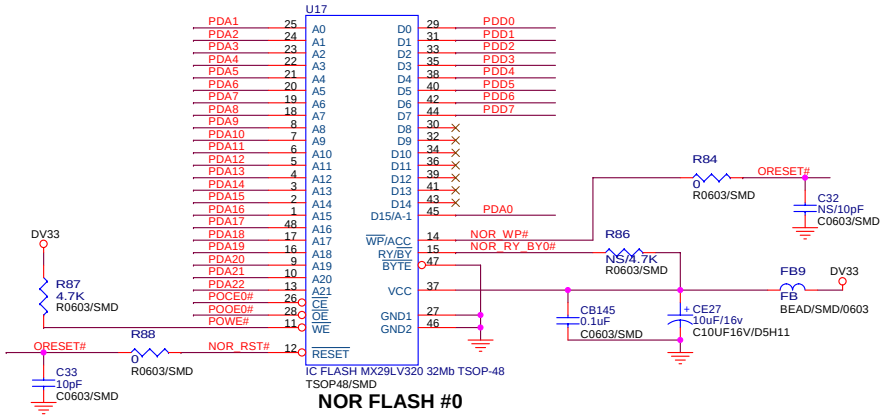


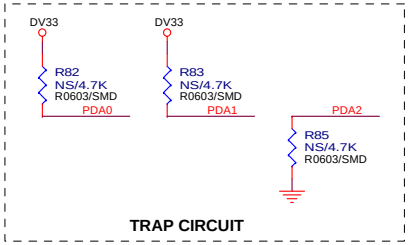
MediaTek Confidential

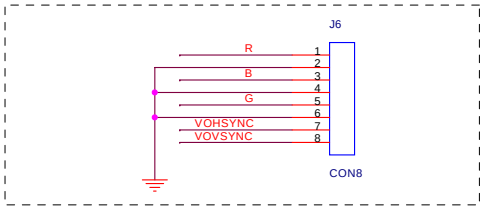
Title: MT5351 PERIPHERAL			
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006		Sheet 6 of 8	

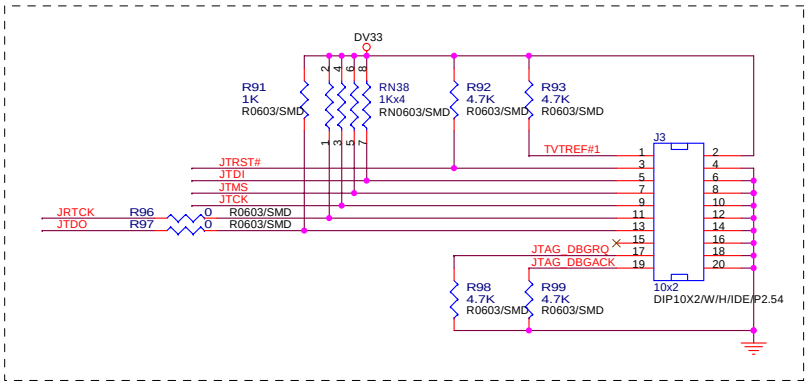


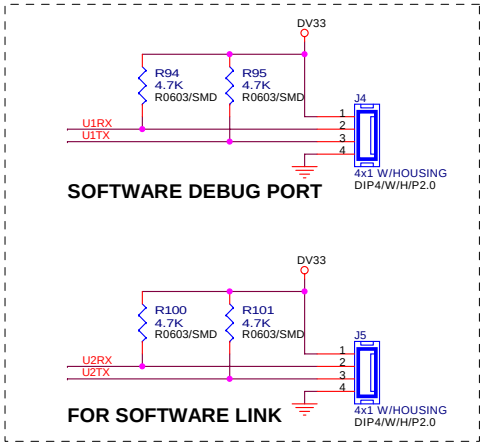
Title	DDR MEMORY		
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006		Sheet 7 of 8	

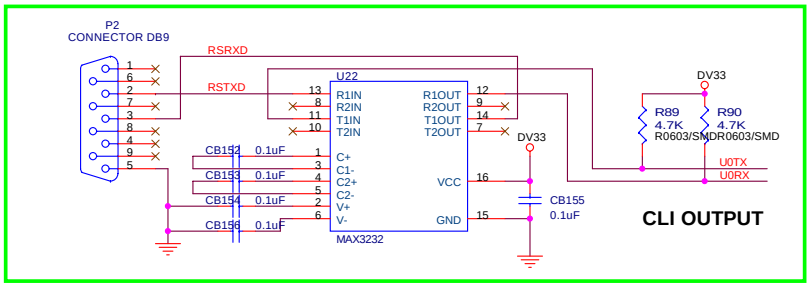


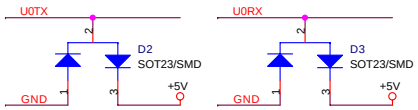


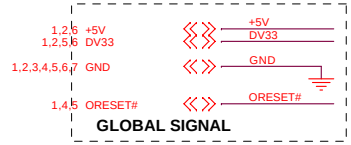


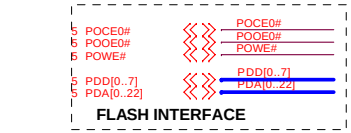


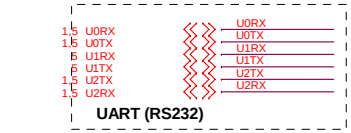












Title	NOR FLASH / JTAG / UART	
Size: Custom	Document Number: MT5351RA-V2	Rev: 1
Date: Monday, February 20, 2006	TwinSon Chan	Sheet 8 of 8

Basic Operations & Circuit Description

MODULE

There are 1 pcs panel and 5 pcs PCB including 3 pcs Extension PCB, 1 pcs Timming controller board and 1 pcs Back Light board in the Module.

SET

There are 6 pcs PCBs including 1 pcs ATV Tuner board, 1 pcs keypad board, 1 pcs Remote Control Receiver board, 2 pcs L/R Speakers and 1 pcs Main(Video)board, 1 pcs ATSC board in the SET.

PCB funtion

1. Power :

   (1). Input voltage: AC 120V, 60Hz.

   (2). To provide power for PCBs.

2. Main board : To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI/HDMI signals and D-SUB signals to digital ones and to transmit to Control board.

3. Control board : Dealing with the digital signal for output to panel.

4. Extension board : Output addressing signals.

5. ATV Tuner Board : To convert TV RF signal to video and SIF audio signal to Main board.

6. ATSC Board : Receiver and converter ATSC TV signal to transmit to main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN : a. Lacking color, Bad color scale.
   b. No voice. (Make sure status: Mute / Internal, External speaker)
   c. No picture but with signals output, OSD and back light.
   d. Abnormal noise on screen.
3. POWER : NO picture, no power output.
4. Back Light : a. No picture.
   b. Flash on screen.
   c. Darker picture with signals.
5. ATV Tuner : a. No ATV Noise
   b. No ATV signals
6. ATSC: a No ATSC TV signal

Main IC Specifications

- M13S128168A (ESMT)
  2M x 16 Bit x 4 Banks Double Data Rate SDRAW

- MT5111CE
  Single-Chip HDTV/CATV Demodulator

- MT8206
  MT8206 is a highly integrated Single-Chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals.

- MT8293
  HDMI PanelLink Cinema Receiver

- R2S15102NP
  Digital Power Amplifier R2S15102NP

- WM8776
  24-bit, 192kHz Stereo CODEC with 5 Channel I/P Multiplexer

MT5111CE
Single-Chip HDTV/CATV Demodulator

Key Features

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -5 to +47*us* range for terrestrial HDTV reception
- On-chip 10-bit ADC for HDTV/CATV demodulator
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- On-chip PLL clock generation
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ±1MHz for ATSC and ±250kHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface
- Controlled by I^2C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-LQFP package
- Lead Free

Functional Block Diagram

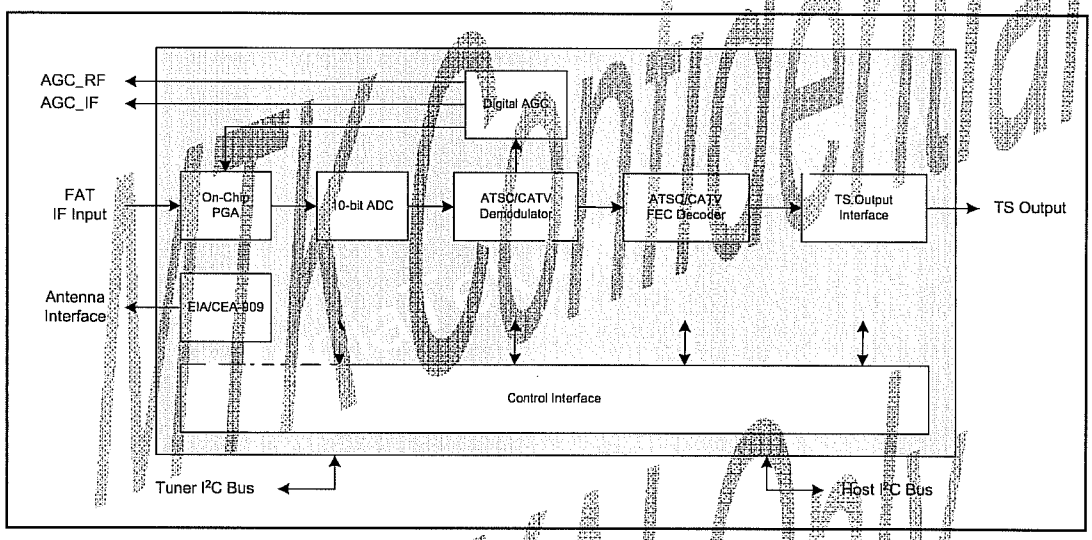


Figure 1: MT5111CE Functional Block Diagram

General Description

MT5111CE is a fully integrated single-chip 8-VSB and 64/256-QAM demodulator. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

MT5111CE includes a 10-bit A/D converter, 8-VSB/QAM demodulator, TCM (Trellis-Coded Modulation) decoder, and Reed-Solomon Forward Error Correction decoder. Moreover, an internal controller handles the acquisition and tracking to ensure the best receiving performance. The internal controller communicates with the external host controller via the I2C-compatible interface, and also provides direct control to the RF tuner via the second I2C-compatible

interface.

MT5111CE accepts either the direct IF signals centered at 44MHz or 43.75MHz, or the low IF signals centered at 5.38MHz. The center frequency of the incoming IF signal can also be programmed to other frequencies for various applications. An On-chip programmable gain-controlled amplifier is designed to provide sufficient signal amplitude when the received RF signal is weak. The IF signal is first sampled by a 10-bit A/D converter. Afterward, the digitized samples are further processed for adjacent channel interference rejection.

MT5111CE measures the power level of the digitized sequence, and feeds the control voltages back to the RF tuner and the IF amplifier respectively. The control voltages are converted to analog signals through the on-chip 1-bit sigma-delta D/A converters plus the off-chip R-C low-pass filters. The automatic gain control keeps the received power level at a desired level and maximizes the received SNR.

The carrier frequency offset and symbol timing offset are both estimated and compensated by a fully digital synchronizer. The synchronizer also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset. All synchronization in MT5111CE are integrated in digital circuits, no external VCXO is required.

The equalizer is adopted to cancel the effect of multi-path fading channel during signal propagation in the air or over cable networks. The equalizer is not only capable of acquiring correct coefficients combination by specified adaptive algorithms, but also programmable to different configurations for various channel conditions.

The following FEC decoder corrects most of the errors by the concatenation

of TCM and Reed-Solomon decoders. For CATV reception, MT5111CE detects and aligns de-puncturing timing of the received sequence. The timing synchronization is also automatically performed to lock the FEC frames. The on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: equalizer output, TCM decoder, and transport stream packets. The chip finally outputs the decoded MPEG-2 packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5111CE also provides the capability to remove the NTSC co-channel interference. To achieve the best reception condition, an antenna interface compliant with EIA/CEA-909 is designed to control the antenna parameters.

MT5111CE is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip controller to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will try to re-acquire the DTV signal automatically.

Pin Out

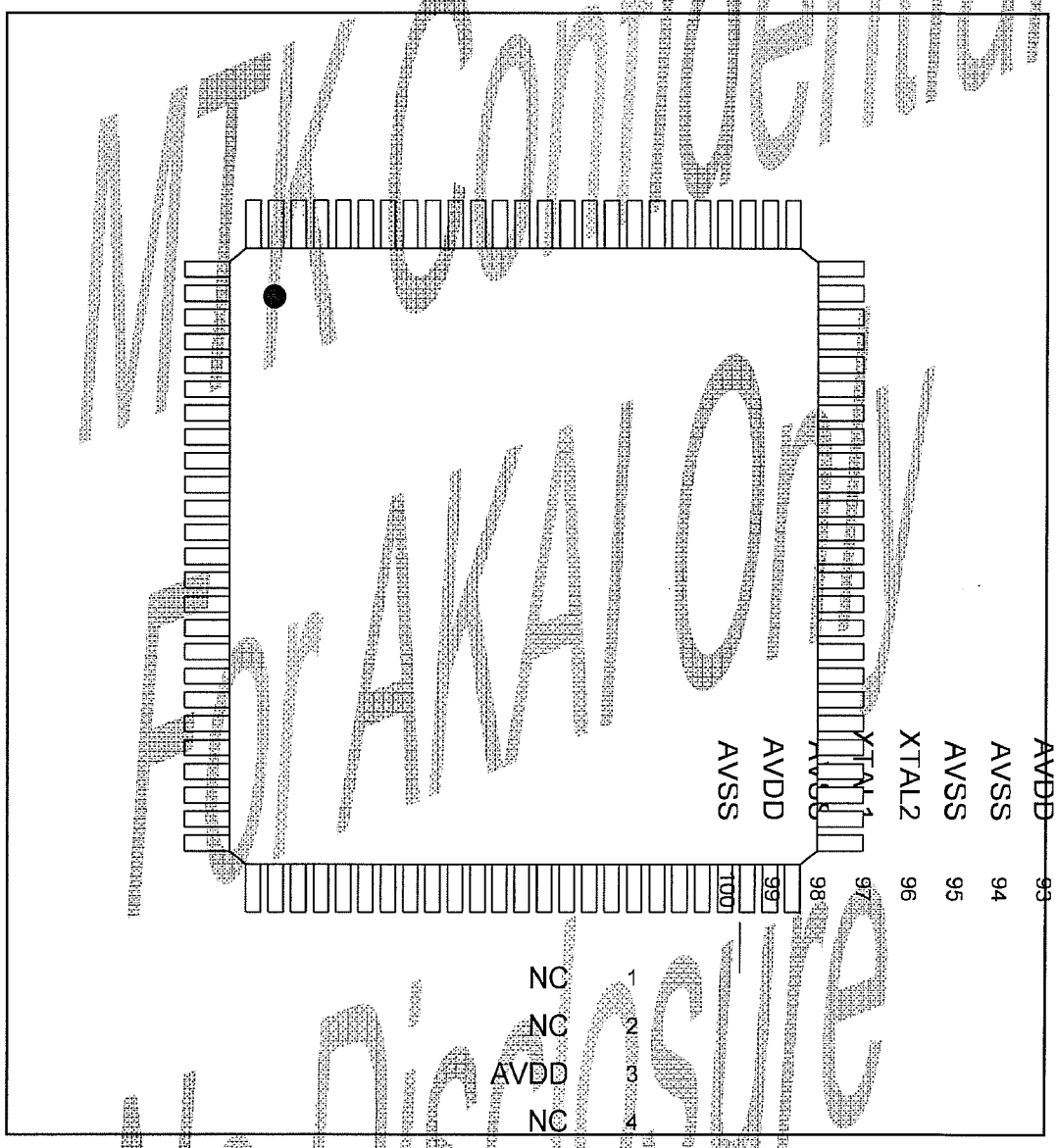


Figure 2: MT5111CE Pin Out

Pin Description

Signal Name	Pin No	I/O	Description
Transport Stream			
TSDATA[7:0]	22,23,24,25,28, 29,32,33,	O	TS data output
TSSYNC	34	O	TS packet start signal
TSVAL	38	O	TS output valid signal
TSCLK	37	O	TS output clock
TSERR	39	O	TS packet error indicator
Analog Signal			
IN+	82	I	Analog differential IF input
IN-	81	I	
REFTOP	88	O	ADC reference top voltage. Decouple with a capacitor to AVSS
REFBOT	86	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
VCMEXT	87	O	ADC common mode voltage
Antenna Interface			
ANTIF	62	O	CEA-909 Antenna Control Interface
Clock Generation			
XTAL1	97	I	25MHz crystal input
XTAL2	96	I	
Control Signals			
HOST_CLK	47	I	Host processor serial clock input, 5 volt compatible
HOST_DATA	44	I/O	Host processor serial data pin, 5 volt compatible
TUNER_CLK	69	O	Tuner serial clock output, 5 volt compatible
TUNER_DATA	68	I/O	Tuner serial data pin, 5 volt compatible
IF_AGC	72	O	IF AGC output
RF_AGC	73	O	RF AGC output
RESET	48	I	Power reset pin, low active
SA0	66	I	Chip slave address selection pin, tie to VDD3.3 or DGND
SA1	67	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
VDD3.3	17,26,35,42, 52,60,70	P	Digital power supply, tie to 3.3V
VDD1.8	18,30,40,45, 55,64,75	P	Digital power supply, tie to 1.8V
DGND	16,19,27,31, 36,41,43,46,51,56, 61,63,65,71,74	P	Digital ground, tie to digital ground plane
AVDD	3,10,12,80,83,91, 92,93,99	P	Analog power supply, tie to 3.3V
AVSS	7,11,79,85,89,94, 95,98,100		Analog ground, tie to analog ground plane
ADVDD3.3	15,76	P	Digital power supply for analog component, tie to 3.3V
AVDD1.8	90	P	Digital power supply for analog component, tie to 1.8V
Others			
NC	1,2,4,5,6,8,9,13,14, 20,21,49,50,53,54, 57,58,59,77,78,84		Not Connected

Table 1: Pin Description

Electrical Characteristic

Recommended Operating Condition

Symbol	Description	Min	Typical	Max	Unit
Tj	Chip Junction Temperature	-	-	125	°C
VDD1.8	1.8V Digital Core Power Supply Voltage	1.62	1.8	1.98	Volt
AVDD	3.3V Analog Power Supply Voltage	3.15	3.3	3.45	Volt
VDD3.3	3.3V Digital IO Power Supply Voltage	3	3.3	3.6	Volt
AVDD1.8	1.8V Analog Power Supply Voltage	1.7	1.8	1.9	Volt
VIH	Digital Input High Voltage	3	3.3	3.6	Volt
VIL	Digital Input Low Voltage	-	0	-	Volt

Table 2: Recommend Operating Condition

Typical Current and Power Dissipation (ASTC Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	350	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	16	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	630	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	52.8	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	917.4	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 3: Typical Current and Power Dissipation (ATSC Mode)

Typical Current and Power Dissipation (QAM Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	175	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	19	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	315	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	62.7	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	612.3	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 4: Typical Current and Power Dissipation (QAM Mode)

MT8206 is a highly integrated single chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals. Embedded HDTV/VGA decoders enable the high quality video reproduction. 24/16/8 bits digital port may accept all kinds of external digital input video source. New 3rd generation advanced motion adaptive de-interlacer converts accordingly the interlace video into progressive non-flicking video. 2D Graphic engine generates high quality UI interface. Advanced full function color processing with fully 10-bit path provides high quality video contents. Independent two Flexible scalars provide wide adoption to various LCD panels for two of different video sources at the same time. Its on-chip audio processor decodes analog signals from tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor reduces the system BOM and shortens the schedule of UI design by high level C program. MT8206 is a cost-effective and high performance HDTV-ready solution to LCD TV product.

FEATURES

- Video Input
  - Support fully programmable 8 Composite/SV input pins
  - Support 2 Component inputs with SDTV format & HDTV 480i/576i/480p/576p/720p/1080i /1080p format
  - Support VGA input up to SXGA (1280x1024x75Hz) including SOG signals
  - Support Digital 24-bit RGB and CCIR 656/601 24/16/8 bit digital input
  - Support Fully Scart function
- TV decoder
  - Full 10-bit data path to enhance the video resolution and reduce digital truncation errors
  - Support PAL (B, G, D, H, M, N, I, Nc), PAL (Nc), PAL, NTSC, NTSC-4.43, SECAM
  - Automatic Luma/Chroma gain control
  - Automatic TV standard detection
  - The 3nd generation NTSC/PAL Motion Adaptive 3D comb filter with huge improvement
  - VBI decoder for Closed-Caption/XDS/ Teletext/WSS/VPS
  - High speed advanced Teletext/Closed-Caption drawing engine directly on OSD plane
  - Macrovision detection
  -
- Video Processor
  - Fully 10-bit processing to enhance the video quality
  - Advanced flesh tone and color processing
  - Gamma/anti-Gamma correction
  - Advanced Color Transient Improvement (CTI)
  - 2D Peaking
  - Advanced horizontal/vertical sharpness
  - Saturation/hue/contrast/Brightness adjustment
  - Black level extender
  - White peak level limiter
  - Adaptive Luma/Chroma management
  - Automatic detect film or video source
  - 3:2/2:2 pull down source detection
  - 3rd generation Advanced Motion adaptive de-interlacing
  - The 3rd generation Advanced 2D/3D Noise reduction for all video paths
  - Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
  - Advanced linear and non-linear Panorama scaling
  - Programmable Zoom viewer
  - Progressive scan output
  - Picture-in-Picture (PIP)
  - Picture-Out-Picture (POP)
  - Advanced dithering processing for LCD display with 6/8/10 bit output
  - Frame rate conversion, 50Hz to 75Hz
- Audio DSP
  - Support BTSC/EIAJ/A2/NICAM decode
  - Stereo demodulation, SAP demodulation
  - Noise reduction
  - Mode selection (Main/SAP/Stereo)
  - Pink noise and white noise generator
  - Equalizer
  - Sub-woofer/Bass enhancement
  - Noise auto mute
  - 3D surround processing include virtual surround
  - Audio and video lip synchronization
  - Support Reverberation
- Audio Input/Output
  - Decode audio AF from Tuner
  - 2 channel audio L/R digital line in
  - 7.1-channel slave digital line in
  - Including full 7.1-channels digital output, 2-channel bypass and 2-channel headphone output
  - Embedded 3 internal DAC output
  - Support 2 independent Audio outputs

- DRAM Controller
  - Supports up to 32M-byte SDR/DDR DRAM
  - Supports 2x16 bit SDR/DDR bus interfaces
  - Build in a DRAM interface programmable clock to optimize the DRAM performance
  - Programmable DRAM access cycle and refresh cycle timings
  - Maximum DRAM clock rate is 175MHz
  - Support 3.3/2.5-Volt SDR/DDR Interface

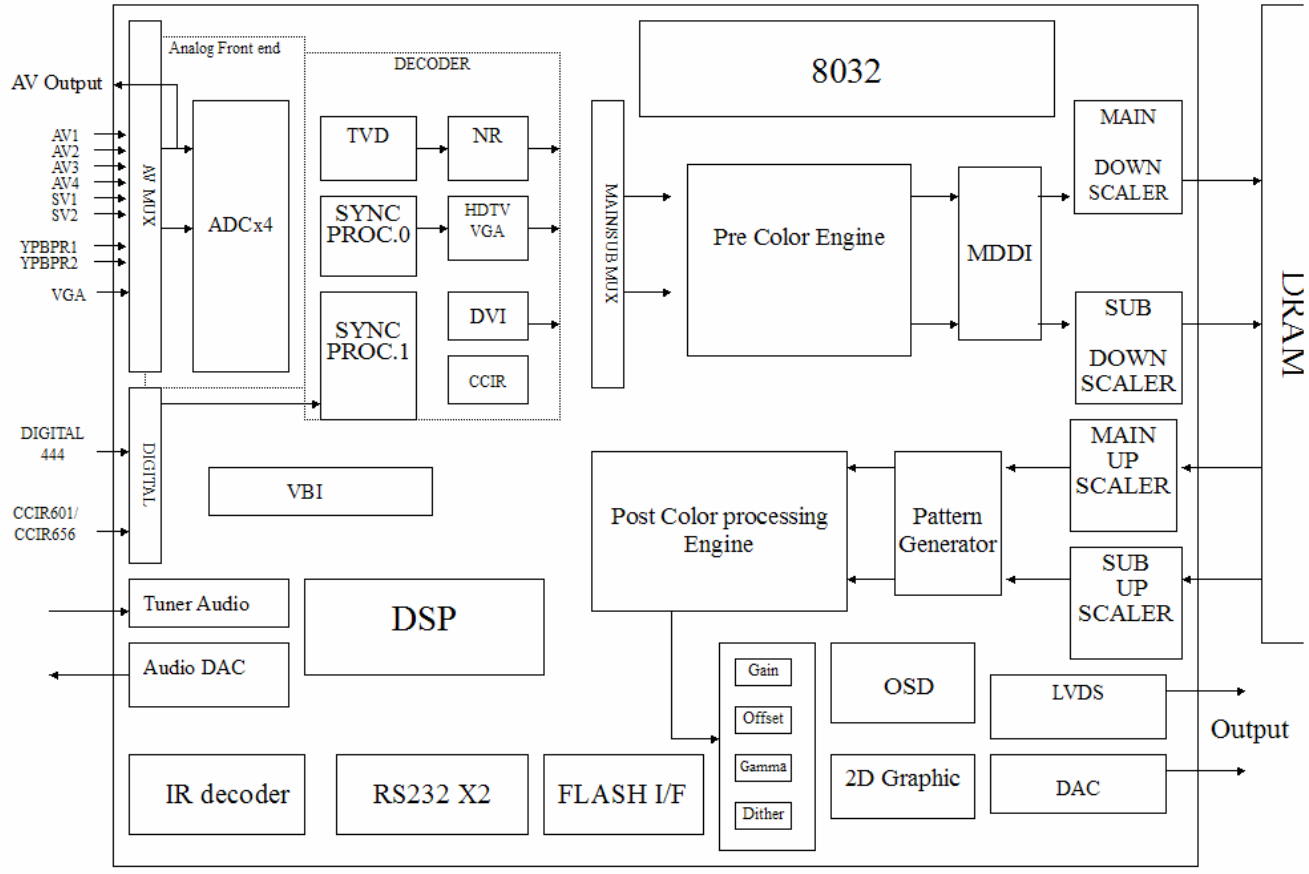
- Video Output
  - Embedded TV pattern generator
  - Interlaced 50Hz to 120Hz
  - Support up to 1080P resolution
  - Dual-channel 6/8/10-bit LVDS output
  - Support video output mirror and upside down

- 2D-Graphic/3 OSD processor
  - Embedded Two backend RGB domain OSD planes and one YUV domain OSD
  - Support Text/Bitmap decoder
  - Support line/rectangle/gradient fill
  - Support bitblt
  - Support color Key function
  - Support Clip Mask
  - Support Alpha blending with video output
  - 65535/256/16/4/2-color bitmap format OSD,
  - Automatic vertical scrolling of OSD image
  - Support OSD mirror and upside down

- Host Micro controller
  - Turbo 8032 micro controller
  - Built-in internal 373 and 8-bit programmable lower address port
  - 2048-bytes on-chip RAM
  - Up to 4M bytes FLASH-programming interface
  - Supports 5/3.3-Volt. FLASH interface
  - Supports power-saving mode
  - Supports additional serial port
  - IR control serial input
  - Support dual RS232 interfaces for external source interface
  - Support 2 PWMs output
  - Support DDC2Bi
  - Programmable GPIOs setting for complex external device control

- Outline
  - 388-pin BGA package
  - 3.3/1.8-Volt. Dual operating voltages
  - 0.18um process

BLOCK DIGRAM



Analog Switch

Analog switches are built in MT8206 to connect to 17 input signals and there is need to add external components to add analog video multiplexes on board.

There are 9 high-speed differential input pairs for 3 sets of YPRPB/VGA input signals.

The 8 Composite/S signal input pins can be fully programmed to connect to any AV/SV inputs.

ADC/ Source Select

The video ADC sample analog input signals. After ADC, all signal processing is digital domain. The source select multiplex all inputs from digital and analog video ports and route them into data path.

Audio Interface

Audio interface accept analog audio signal from Tuner, e.g. AF. It also includes preprocessing circuit to filter the noisy audio signals. Audio decoder will decode the BTSC or NICAM, and output best sound with enhanced 3D surround post-processing.

Embedded 7.1 channel digital audio input (slave) and 2 channels (master) digital audio inputs.

Embedded 3 high performance audio DACs.

DSP

DSP handle audio decoding as well as computing intensive jobs. The downloadable micro code enables fast function convergence for various audio standards in the world.

Advanced DSP engine supports full functions of sound effects.

Support Dolby Surround and WOW SRS

MDDi/Scaler

MDDi is MTK proprietary de-interlacing technology. The 3rd generation MDDi solution provides improved low angle processing and more accurate motion detection for all interlace sources. The techniques reduce jagged edges and broken images. The MDDi engine supports both Main and Sub channel SDTV inputs or one channel 1080i high quality de-interlacing.

Two totally independent scalers support full functions of PIP/POP and frame rate conversion.

With MDDi and high quality scaler, MT8206 guarantee all input format could be translated to output format with best video quality for motion and still pictures.

Color/Gamma

MT8206 provides advanced color management engine for user to improve video quality with fully flexibility. With contrast/hue/saturation/Gamma/anti-Gamma/flesh tone function, and well algorithm control, MT8206 deliver the best video quality with vivid color.

Advanced dither function support 6/8/10-bit video output for any kinds of display unit (LCD, PDP, CRT).

8032

On-chip Turbo8032 provide the most cost effective development environment for system house. Well-proven F/W could speed up the system design significantly.

2D-G/OSD

On-chip graphic engine draw bitmap OSD and store them into DRAM. OSD read data from DRAM and display on screen. With 2D-G and OSD. The computing power requirement of μP will be minimized.

MEDIATEK

MT8293

Specifications are subject to change without notice

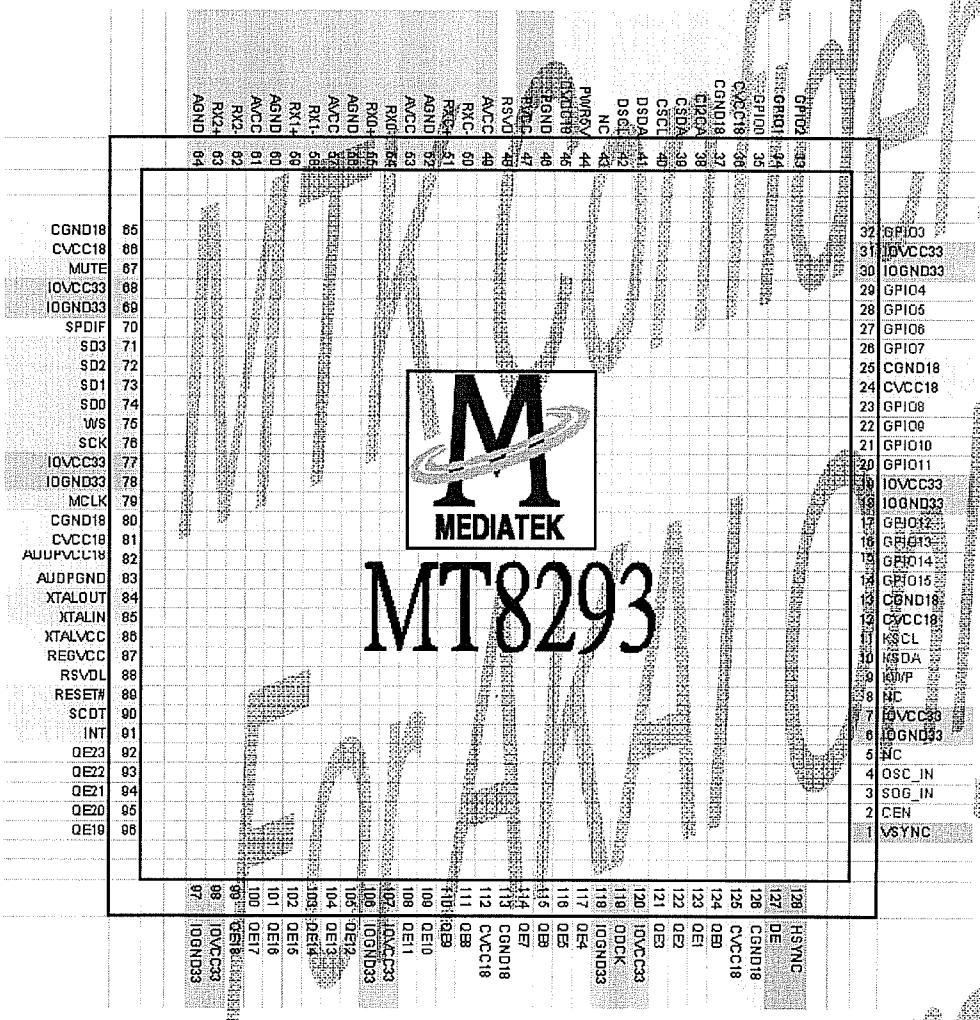
HDMI PanelLink Cinema Receiver

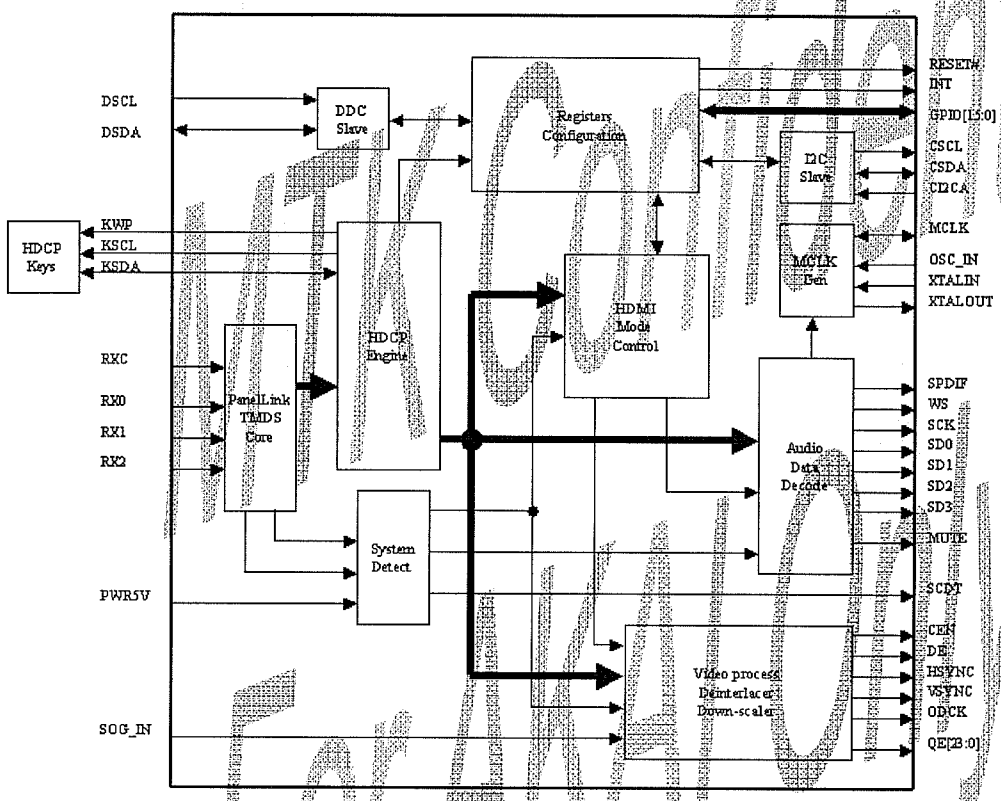
MT8293 is a low-cost, fully HDMI-compliant receiver that fits directly into home theater products such as LCD TVs, plasma TVs and HDTVs. The receiver is capable of supporting bandwidths up to 165MHz and video resolutions up to 1080p and UXGA. The MT8293 supports the DVD-Audio standard, including 7.1- surround audio at 96kHz and stereo audio at 192kHz.

The built-in High-bandwidth Digital Content Protection (HDCP) decryption engine secures the digital link for transmission of valuable high-definition video and audio.Built-in HDCP self-test engine simplifies manufacturing testing.

FEATHRES

- Industry-Standard
  - HDMI 1.1
  - DVI 1.0
  - EIA/CEA-861B
  - HDCP 1.1
- Digital Video Output
  - Integrated PanelLink Core
  - Supports DTV (480i/576i/480p/576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/UXGA) resolution up to 165MHz (using dual edge to transmit video data for pixel clock over 112MHz)
  - Flexible digital video interface
    - 24-bit RGB/YCbCr 4:4:4
    - 16-bit YCbCr 4:2:2
    - 8-bit YCbCr 4:2:2 (ITU-R BT.656)
  - Integrated RGB <-> YCbCr color space conversion (both 601 and 709)
  - 4:2:2 <-> 4:4:4 converter
  - Integrated Deinterlacer for 480i/576i (SDTV only)
  - Integrated Down-Scaler (with CEN)
- Digital Audio Output
  - Industry-standard S/PDIF and 3-wire output
  - Supports high-end audio including DVD-Audio
    - 2-ch. 32-192kHz or
    - 8-ch. 32-96kHz
  - Programmable 3-wire output supports numerous low-cost I2S audio DACs
  - Supports IEC60958 2-channel PCM
  - Capable of carrying IEC61937 compressed audio (Dolby Digital, DTS, etc.)
- Content Protection
  - Integrated HDCP cipher engine
  - External EEPROM for encrypt HDCP keys
  - Built-in HDCP self-test
  - Decrypts both video and audio
- System Operation
  - Register-programmable via slave I2C interface
  - Auto video mode
  - Auto audio mode
  - Flexible interrupt registers with interrupt pin
- Power Management
  - 1.8V core provides low-power operation
  - Flexible power-down modes
- Outline
  - 128-pin QFP package





Item	Symbol	Pin #	Type	Description
DIGITAL				
Power/Ground (45)				
1	CVCC18	12,24,36,45,66,81,112,125	I	Digital Logic 1.8V power
2	CGND18	13,25,37,65,80,113,126	I	Digital Logic ground
3	IOVCC33	7,19,31,68,77,98,107,120	I	Input/Output Pin 3.3V power
4	IOGND33	6,18,30,69,78,97,106,118	I	Input/Output Pin ground
5	AVCC	49,53,57,61	I	TMDS Analog 3.3V power
6	AGND	52,56,60,64	I	TMDS Analog ground
7	PVCC	47	I	TMDS PLL 3.3V power
8	PGND	46	I	TMDS PLL ground
9	AUDPVCC18	82	I	ACR PLL 1.8V power
10	AUDPGND	83	I	ACR PLL ground
11	XTALVCC	86	I	ACR PLL crystal input 3.3V power
12	REGVCC	87	I	ACR PLL regulator 3.3V power
Configuration/Programming (20)				
1	INT	91	O	Interrupt output
2	RESET#	89	I	Reset Pin. Active low
3	DSCL	42	I	DDC I2C clock, 5V tolerance
4	DSDA	41	I/O	DDC I2C data, 5V tolerance
5	CSCL	40	I	Configuration I2C clock
6	CSDA	39	I/O	Configuration I2C data
7	KSCL	11	O	KEYS EEPROM I2C clock
8	KSDA	10	I/O	KEYS EEPROM I2C data
9	KWP	9	O	KEYS EEPROM write protect
10	SCDT	90	O	Indicates active video at HDMI input port
11	CISCA	38	I	I2C device address select

Item	Symbol	Pin #	Type	Description
12	PWR5V	44	I	TMDS port transmitter detect (hot plug), 5V tolerance
13	RSVDL	88	I	Must be tied low
14	RSVD	48	O	
15	NC	43	-	No connect
16	NC	8,5	-	No connect
17	OSC_IN	4	I	Oscillator input, External in
18	SOG_IN	3	I	SOG input, External AD in
19	CEN	2	O	Clock enable, for 8202 CEN input
Digital Audio Interface (9)				
1	MCLK	79	I/O	Audio master clock input reference
2	SCK	76	O	I2S serial clock output
3	WS	75	O	I2S word select output
4	SD0	74	O	I2S serial data output
5	SD1	73	O	I2S serial data output
6	SD2	72	O	I2S serial data output
7	SD3	71	O	I2S serial data output
8	SPDIF	70	O	S/PDIF audio output
9	MUTE	67	O	Mute audio output
GPIO Interface (16)				
1	GPIO0	35	I/O	GPIO
2	GPIO1	34	I/O	GPIO
3	GPIO2	33	I/O	GPIO

Item	Symbol	Pin #	Type	Description
4	GPIO3	32	I/O	GPIO
5	GPIO4	29	I/O	GPIO
6	GPIO5	28	I/O	GPIO
7	GPIO6	27	I/O	GPIO
8	GPIO7	26	I/O	GPIO
9	GPIO8	23	I/O	GPIO
10	GPIO9	22	I/O	GPIO
11	GPIO10	21	I/O	GPIO
12	GPIO11	20	I/O	GPIO
13	GPIO12	17	I/O	GPIO
14	GPIO13	16	I/O	GPIO
15	GPIO14	15	I/O	GPIO
16	GPIO15	14	I/O	GPIO
TTL Interface (28)				
1	DE	127	O	Data enable
2	VSYNC	1	O	Vertical sync
3	HSYNC	128	O	Horizontal sync
4	ODCK	119	O	Output data clock
5	QE0	124	O	24-bit Even pixel
6	QE1	123	O	24-bit Even pixel
7	QE2	122	O	24-bit Even pixel

Item	Symbol	Pin #	Type	Description
8	QE3	121	O	24-bit Even pixel
9	QE4	117	O	24-bit Even pixel
10	QE5	116	O	24-bit Even pixel
11	QE6	115	O	24-bit Even pixel
12	QE7	114	O	24-bit Even pixel
13	QE8	111	O	24-bit Even pixel
14	QE9	110	O	24-bit Even pixel
15	QE10	109	O	24-bit Even pixel
16	QE11	108	O	24-bit Even pixel
17	QE12	105	O	24-bit Even pixel
18	QE13	104	O	24-bit Even pixel
19	QE14	103	O	24-bit Even pixel
20	QE15	102	O	24-bit Even pixel
21	QE16	101	O	24-bit Even pixel
22	QE17	100	O	24-bit Even pixel
23	QE18	99	O	24-bit Even pixel
24	QE19	96	O	24-bit Even pixel
25	QE20	95	O	24-bit Even pixel
26	QE21	9	O	24-bit Even pixel
27	QE22	93	O	24-bit Even pixel
28	QE23	92	O	24-bit Even pixel

Item	Symbol	Pin #	Type	Description
ANALOG (8)				
Differential signal				
1	RXC+	51	I	TMDS input clock pair
1	RXC-	50	I	TMDS input clock pair
1	RX0	55	I	TMDS input data pair
1	RX0	54	I	TMDS input data pair
1	RX1	59	I	TMDS input data pair
1	RX1	58	I	TMDS input data pair
1	RX2	63	I	TMDS input data pair
1	RX2	62	I	TMDS input data pair
PLL group(2)				
68	XTALIN	85	I	Crystal input PAD
69	XTALOUT	84	O	Crystal output PAD

MEDIATEK

MT5351

Specifications are subject to change without notice.

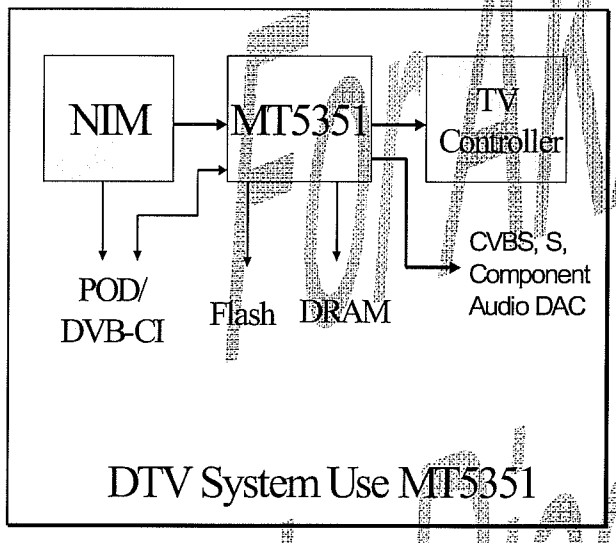
DTV Backend Decoder SOC

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, JPEG decoder, MPEG1,2, MP3, AC3 audio decoder, HD TV encoder. The MT5351 enables consumer electronics manufactures to build high quality, feature-rich DTV, STB or other home entertainment audio/video device.

World-Leading Technology: HW support worldwide major broadcast network and CA standards, include ATSC, DVB, OpenCable, DirectTV, MHP.

Rich Feature for high value product: To enrich the feature of DTV, the MT5351 support 1394-5C component to external DVHS. Dual display, PIP/POP and quad pictures provide user a whole new viewing experience.

Credible Audio/Video Quality: The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. The embedded 4X over-sample video DAC could generate very fine display quality. Also, the audio 3D surround and equalizer provide professional entertainment



DTV System Use MT5351

Key Features:

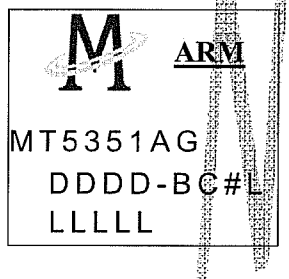
1. Flexible Demuxer
2. Dual HD MPEG2 Video Decoder
3. Dual MPEG1,2, MP3, AC3 Audio decode
4. Dual Display
5. PIP/POP/Quad Mode
6. IEEE1394-5C
7. POD/DVB-CI

Application:

1. DTV
2. Set-top Box
3. DTV Recorder
4. Home Media Center

Order Information:

MT5351AG → one HD decoder
MT5351CG → two HD decoder
All Package are Lead Free



IC Top View:

DDDD: Date Code
#: Subcontractor Code
LLLLL: Lot Number

General Feature List

- Host CPU
  - ARM 926EJ
  - 16K I-Cache and 16K D-Cache
  - 8K Data TCM and 8K Instruction TCM
  - JTAG ICE interface
  - Watch Dog timers
- Transport Demuxer
  - Support 3 independent transport stream inputs.
  - Support serial / parallel interface for each transport stream input.
  - Support ATSC, DVB, and MPEG2 transport stream inputs.
  - Programmable sync detection.
  - Support DES/3-DES de-scramble
  - 96 PID filter and128 section filters.
  - Support TS recording via IEEE1394 interface
- MPEG2 Decoder
  - Support dual MPEG-2 HD decoder or up to 8 SD decoder
  - Complaint to MP@ML, MP@HL and MPEG-1 video standards
- JPEG Decoder
  - Decode Base-line or progressive JPEG file
- 2D Graphics
  - Support multiple color modes
  - Point, horizontal/vertical line primitive drawing
  - Rectangle fill and gradient fill functions
  - BitBlt with transparent, alpha blending, alpha composition and stretch
  - Font rendering by color expansion
  - Support clip masks
  - YCbCr to RGB color space transfer
- OSD Display
  - 3 linking list OSDs with multiple color mode
  - OSD scaling with arbitrary ratio from 1/2x to 2x
  - Square size, 32x32 or 64x64 pixel, hardware cursor
- Video Processing
  - Advanced Motion adaptive de-interlace on SDTV resolution
  - Support clip
  - 3:2/2:2 pull down source detection
  - Arbitrary ratio vertical/horizontal scaling of video, from 1/15X to 16X
  - Support Edge preserve
  - Support horizontal edge enhancement
  - Support Quad-Picture
- Main Display
  - Mixing two video and three OSD and hardware cursor
  - Contrast/Brightness adjustment
  - Gamma correction
  - Picture-in-Picture (PIP)
  - Picture-Out-Picture (POP)
  - 480i/576i/480p/576p/720p/1080i output
- Auxiliary Display
  - Mixing one video and one OSD
  - 480i/576i output
- TV Encoder
  - Support NTSC M/N, PAL M/N/B/D/G/H/I
  - Macrovision Rev 7.1.L1
  - CGMS/WSS
  - Closed Captioning
  - Six12-bit video DACs for CVBS, S-video or RGB/YPbPr output
- Digital Video Interface
  - Support SAV/EAV
  - Support 8/16 for SD/HD digital video input
  - Support 8/16/24 bits digital output for main display
  - Support 8 bits digital output for aux display
- DRAM Controller
  - Supports 64Mb to 1Gb DDR DRAM devices
  - Configurable 32/64 bit data bus interface
  - Support DDR266, DDR333, DDR400 JEDEC specification compliant SDRAM
- Peripheral Bus Interface
  - Support NOR/NAND flash
  - Support CableCard host control bus
- Audio

- Support Dolby Digital AC-3 decoding
- MPEG-1 layer I/II, MP3 decoding
- Dolby prologic II
- Main audio output: 5.1ch + 2ch (down mix)
- Auxiliary audio output: 2ch
- Pink noise and white noise generator
- Equalizer
- Bass management
- 3D surround processing include virtual surround
- Audio and video lip synchronization
- Support reverberation
- SPDIF out
- I2S I/F

■ Peripherals

- Three UARTs with Tx and Rx FIFO, two of them have hardware flow control
- Two serial interfaces, one is master only; the other can be set to master mode or slave mode
- Two PWMs
- IR blaster and receiver
- IEEE 1394 link controller
- IDE bus: ATA/ATAPI7 UDMA mode 5, 100 MB/s
- Real-time clock and watchdog controller
- Memory card I/F: MS/MS-Pro, SD, CF, and MMC
- PCMCIA/POD/CI interface

■ IC Outline

- 471 Pin BGA Package
- 3.3V/1.2V dual Voltage

Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameters	Value	Unit
IOVDD	3.3V supply voltage	-0.5 to 4.6	V
CVDD	1.2V supply voltage	-0.5 to 1.8	V
AVDD	Analog supply voltage	-0.5 to 4.6	V
RVDD	DDR supply voltage	-0.5 to 3.5	V
VIN(3.3V)	Input Voltage(3.3V IO)	VSS-1.0 to 3.63	V
VIN(5V tolerance)	Input Voltage(5V tolerance IO)	VSS-1.0 to 5.5	V
Vout	Output Voltage	-0.3 to VDD3+0.3	V
Ts	Storage Temperature	-40 to 150	C
Ta	Ambient Temperature	0 to 70	C

DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
IOVDD	3.3V supply voltage	2.97	3.3	3.63	V
CVDD	1.2V supply voltage	1.08	1.2	1.32	V
AVDD	Analog supply voltage	2.97	3.3	3.63	V
VIH(3.3V)	3.3V input voltage high	2.0			V
VIL(3.3V)	3.3V input voltage low			0.8	V
VOH(3.3V)	3.3V output voltage high	2.4			
VOL(3.3V)	3.3V output voltage low			0.4	
VIH(3/5V)	3/5V tolerance input voltage high	2.0			V
VIL(3/5V)	3/5V tolerance input voltage low			0.8	V
VOH(3/5V)	3/5V tolerance output voltage high	2.4			V
VOL(3/5V)	3/5V tolerance output voltage low			0.4	V
Tj	Junction operation temperature	-40	25	125	C
PD(estimate)	Power dissapation		1.5		W
Pdown	Power down mode		2		mW

DDR ELECTRICAL Characteristics and DC Operating Condiction

Symbol	Parameters	Min	Typ	Max	Unit
RVDD(DDR333)	DDR I/O supply voltage for DDR266 or DDR333	2.3	2.5	2.7	V
RVDD(DDR400)	DDR I/O supply voltage for DDR400	2.5	2.6	2.7	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.15		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.15	V

DDR AC Operating Condiction

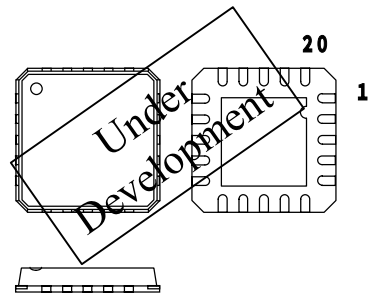
Symbol	Parameters	Min	Typ	Max	Unit
VIH	Input high voltage, DQ, DQS	DVREF+0.31			V
VIL	Input low voltage, DQ, DQS			DVREF-0.31	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.5	V

10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1.Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.
R2S15102NP can realize maximum Power 10W × 2ch
(VD = 24V,THD = 10%, SE) at 8 Ω load.
It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

Fig. 1 Package



20pin QFN
Body : 6 x 6 mm
Lead pitch : 0.8 mm

2.Feature

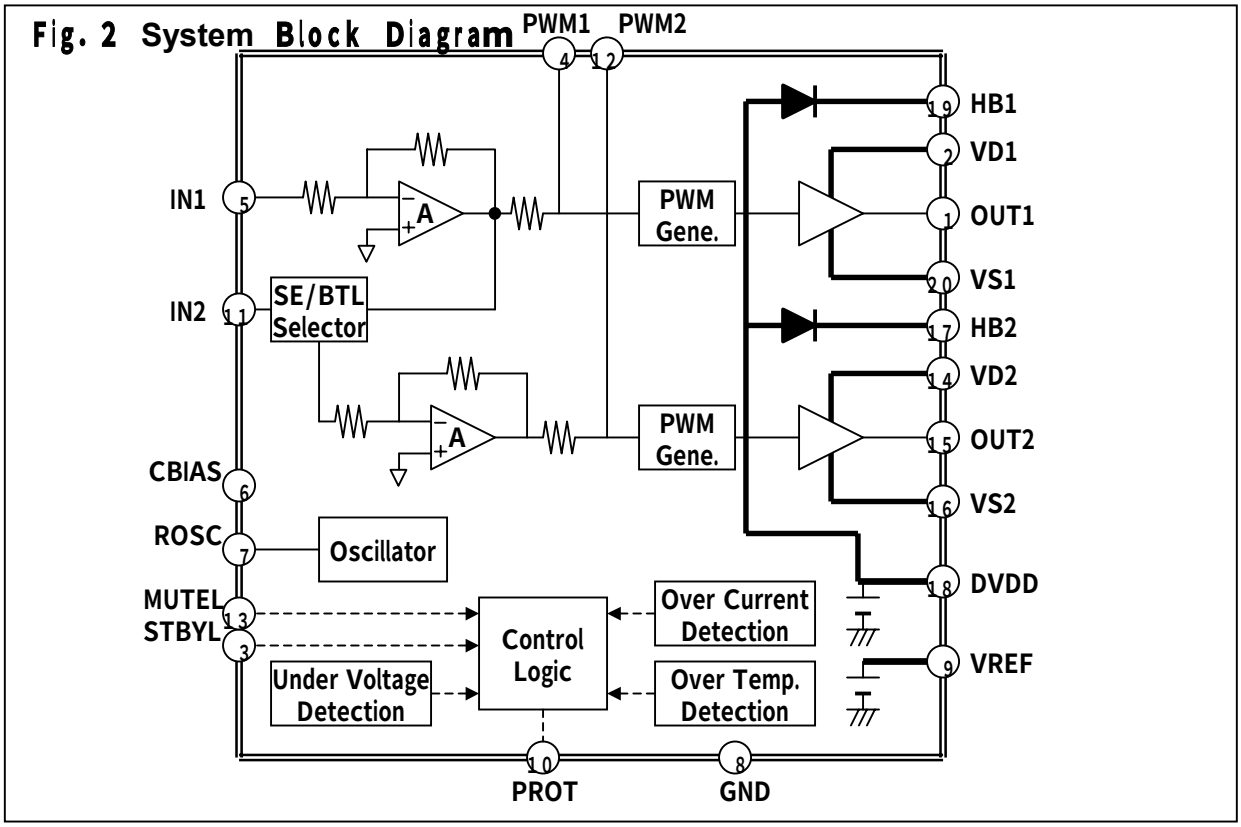
- **High** Output Power(THD=10%)**without external Heat Sink**
  (note) the thermal pad is soldered the thermal pad with the printed-circuit board directly.
  Recommanded Power Condition
  SE operation mode :10Wx2ch(VD=24V) at 8 Ω
  BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω
- The RENESAS original circuits realize high power efficiency, low noise and low distortion characteristics.
- **Pop sound Less**
- **Built-in protection function**
  (Over Current, Over Temperature and Under Voltage)
- **Built-in Mute and Stand-by function**

3.Operating Condition

- **Recommanded** Power supply voltage : **from 11V to 25V**
- **Recommanded** Speaker Impedance : from 4 to 8Ω

4.Block Diagram

Fig. 2 System Block Diagram



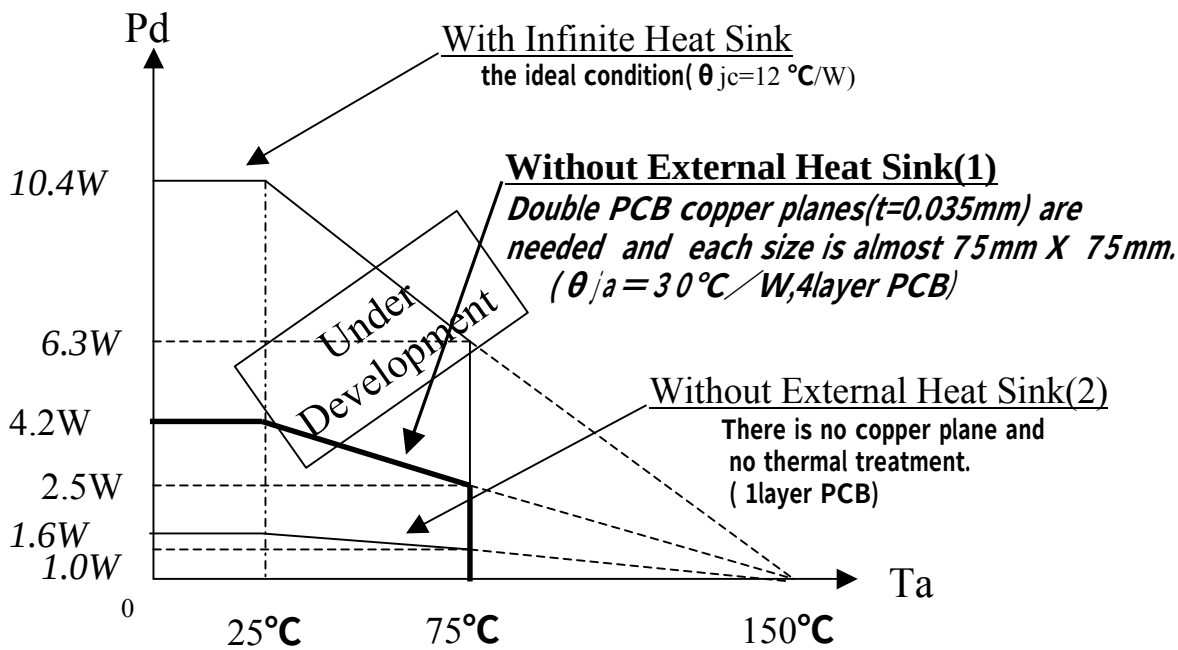
5. Pin Configuration(Table.1)

No.	NAME	I/O	Description	
1	OUT1	O	Power Output pin #1	
2	VD1	—	Power supply pin for power output stage #2	
3	STBYL	I	Stand-by control pin. When this is “L”, circuit current is reduced.There is the pull-down resistor:50Kohm(typ.).	
4	PWM1	I	PWM input pin #1 (for phase compensation)	
5	IN1	I	Analog input #1. The gain is depended on the external resistance .	
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	ROSC	I	Control pin for PWM carrier frequency	
8	GND	—	GND pin for analog block	
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source	
10	PROT	O	Protection Timer pin. At protection mode,the output becomes “L”-level. (The timing capacitor is connected)	
11	IN2	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resister, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 (for phase compensation)	
13	MUTEL	I	Mute control pin. When this is “L”, it becomes mute status.	
14	VD2	—	Power supply pin for power output stage #2	
15	OUT2	O	Power Output pin #2	
16	VS2	—	Ground pin for power output stage #2	
17	HB2	I/O	Capacitor connection pin for bootstrap	
18	DVDD	O	Built-in power supply pin for internal digital block.	
19	HB1	I/O	Capacitor connection pin for bootstrap #1	
20	VS1	—	Ground pin for power output stage #1	

6. Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1、HB2 pin voltage	40	V
Pd	Power dispassion	Ta = 25°C :See Fig.3	4.2	W
θja	Thermal Resistance	See Fig.3	30	℃/W
Tj	Junction temperature	Maximum Temperature	150	℃
Ta	Operating ambient temperature	Temperature range	-20～75	℃
Tstg	Storage temperature	Temperature range	-40～150	℃

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

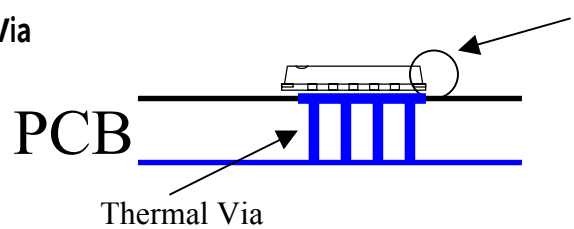


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is directly soldered with the printed-circuit board pattern .

(2)Thermal Via



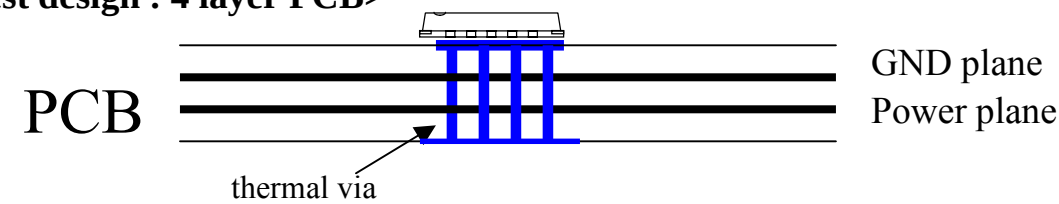
(caution)
There are side expositions of the die pad at corners of the package.
(The die pad is grounded.)

Consideration about the PCB design

The Power dispassion at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at θja=30℃/W.

(1)PCB basic design (copper plane)

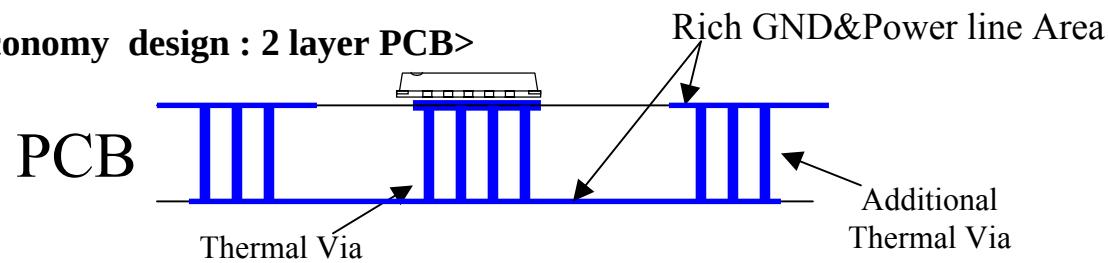
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



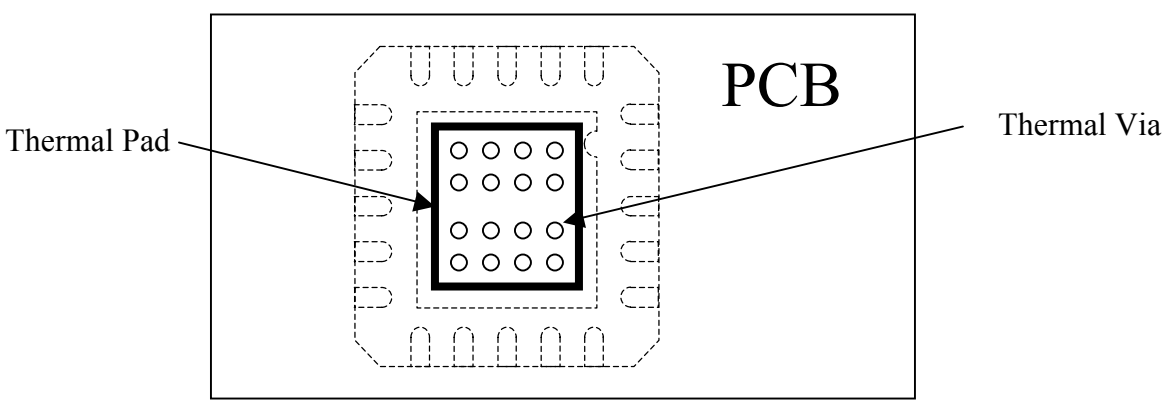
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+α)mm x (75+α) mm

(2)PCB Thermal Pad

The exposed die pad is directly soldered with the printed-circuit board pattern .



7. Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL、MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL、MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33kΩ	300	400	600	kHz

(note) ・STBYL: High level:normal operation Low level:Stand-by
・MUTEL:High level:normal operation Low level:Mute
・The carrier frequency can be changed by the resistance at Pin#.7 .

8. Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	℃
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	℃
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%、VD=24V、RL=8Ω	TBD	10	-	W/ch
		at BTL	THD=10%、VD=18V、RL=8Ω	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100Hz	TBD	50	-	dB

9. Application Examples

(note)
"R for GND" 's are for the evaluation only and not needed actually.

Fig.4 SE operation mode(10Wx2ch)

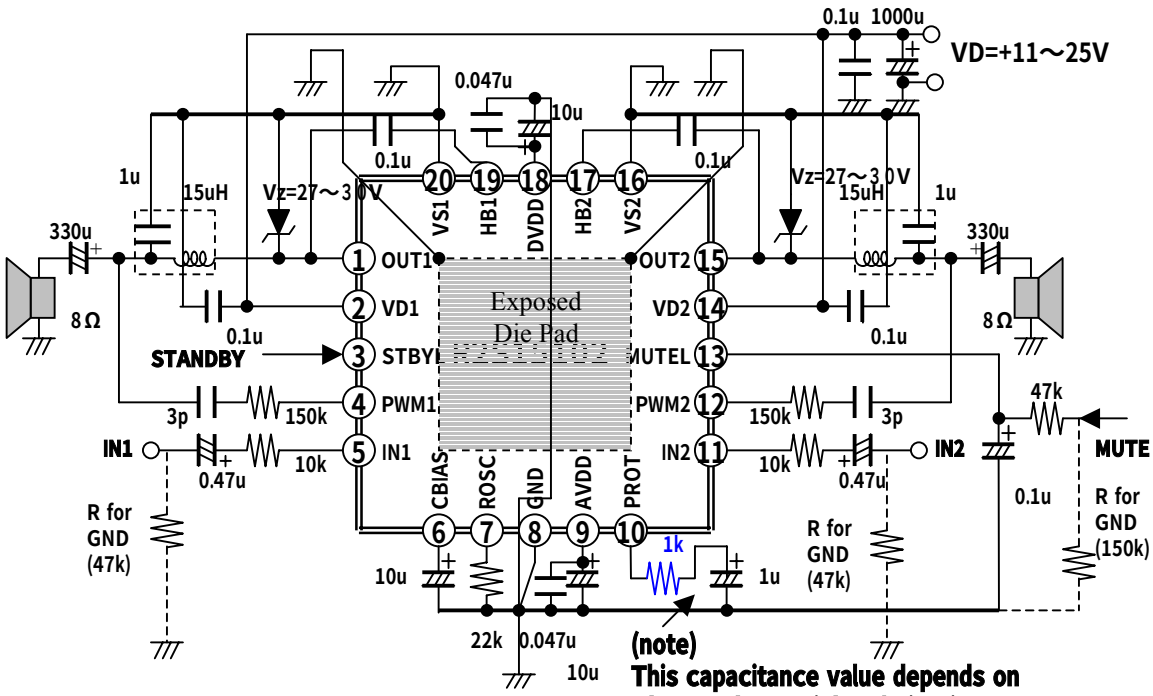


Fig.5 BTL operation mode (20W)

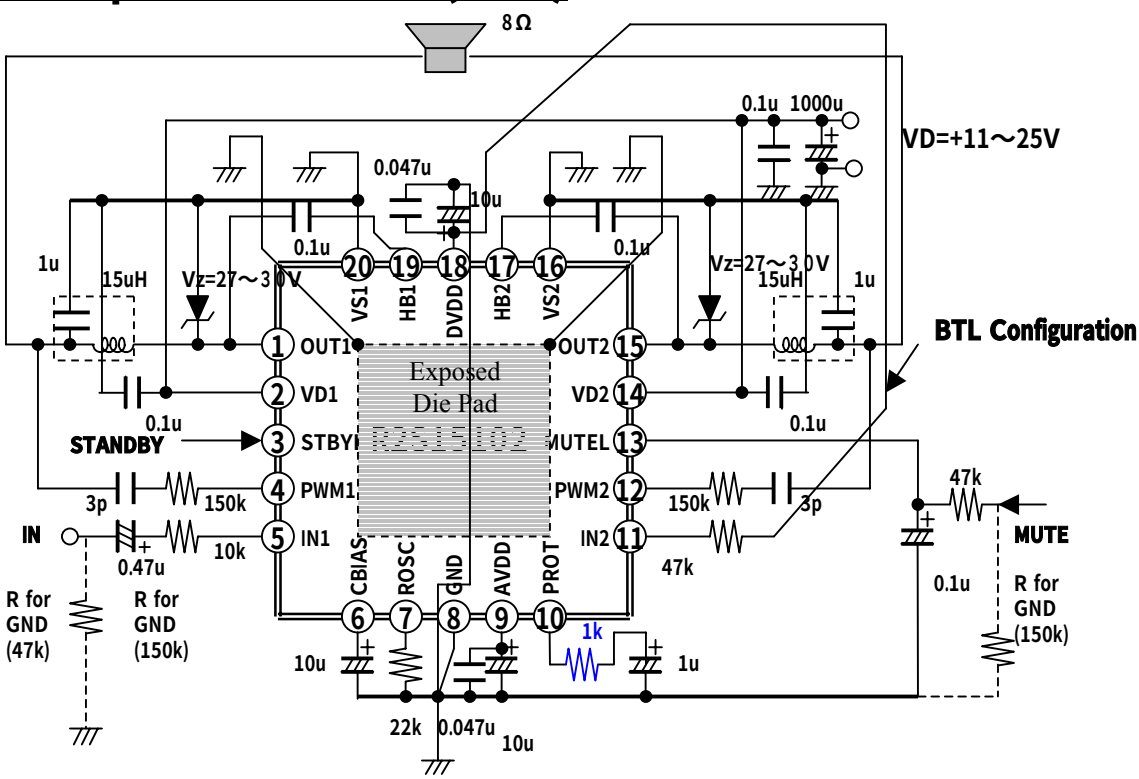


Fig.6 BTL operation mode(20W) with PWM direct input

(note)
"R for GND" 's are for the evaluation only and not needed actually.

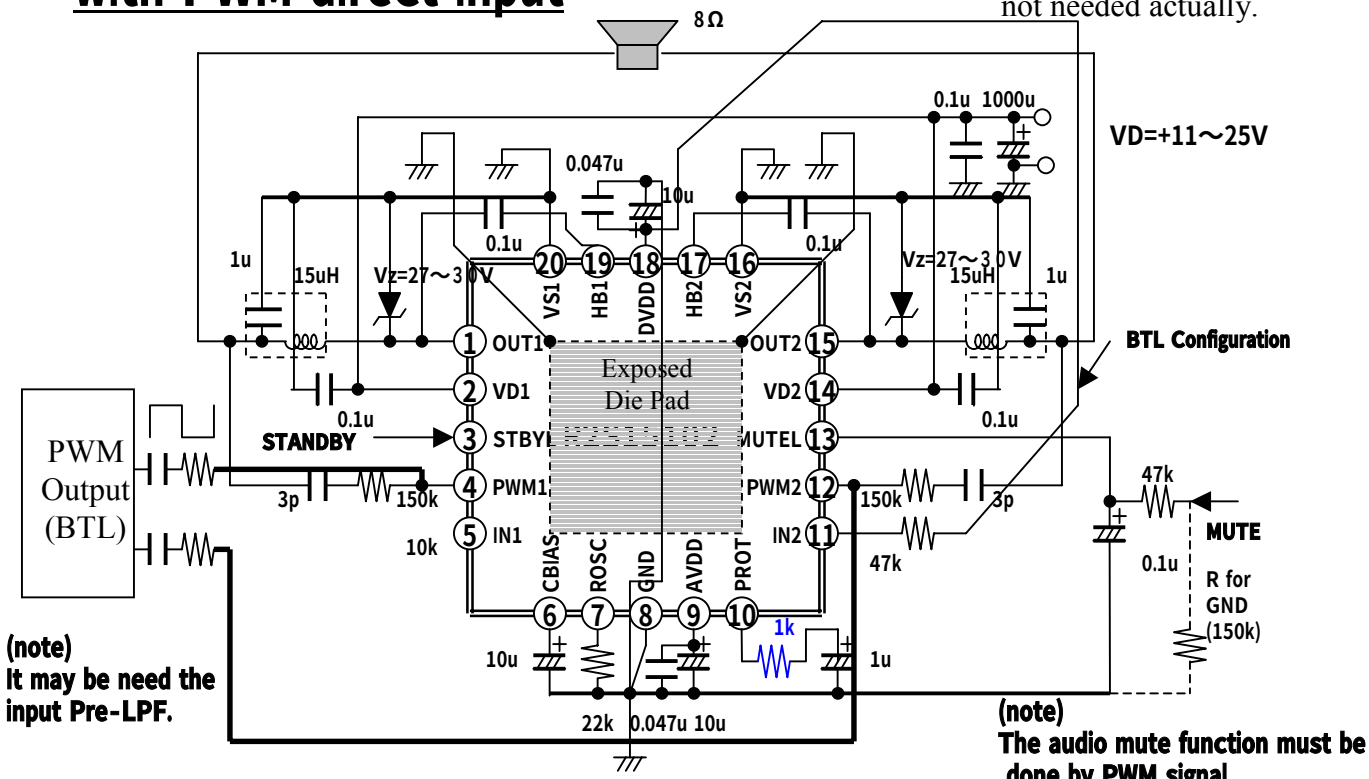
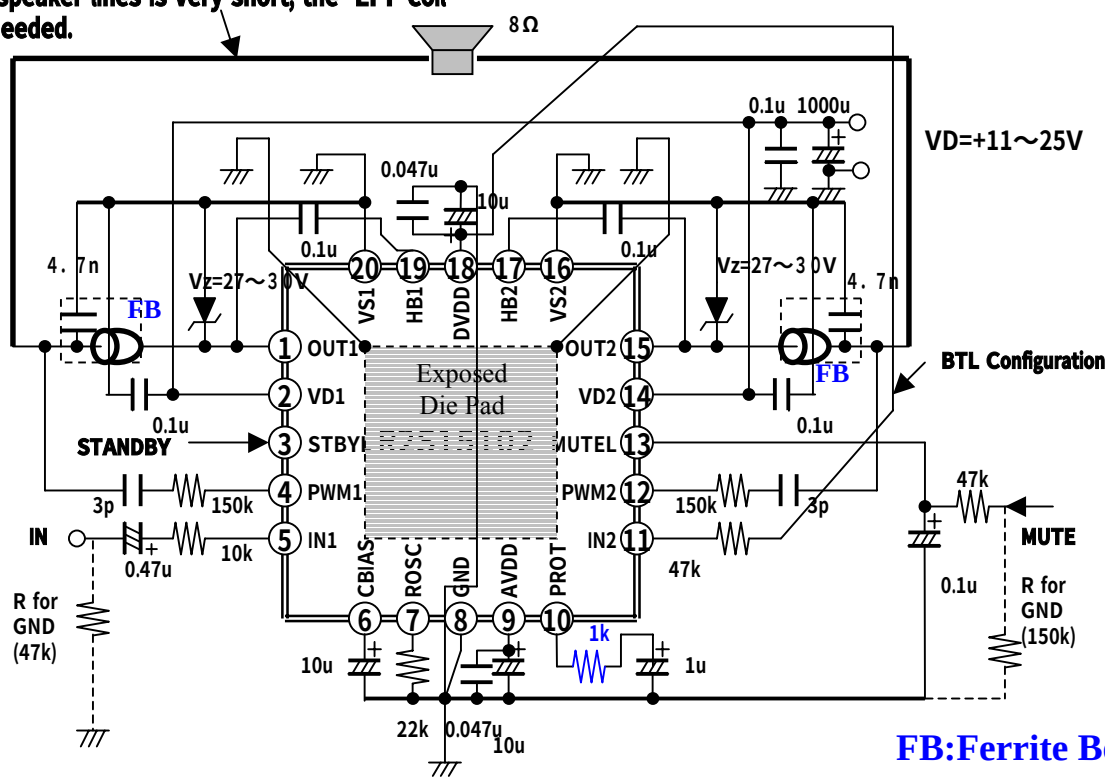


Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil is not needed.



WM8776

24-bit, 192kHz Stereo Codec with 5 Channel I/P Multiplexer

DESCRIPTION

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a five stereo channel input mixer. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

A stereo 24-bit multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with volume controls for the headphones.

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I^2S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface, selected by the MODE pin, which provides access to all features including channel selection, volume controls, mutes, and de-emphasis facilities.

The device is available in a 48-pin TQFP package.

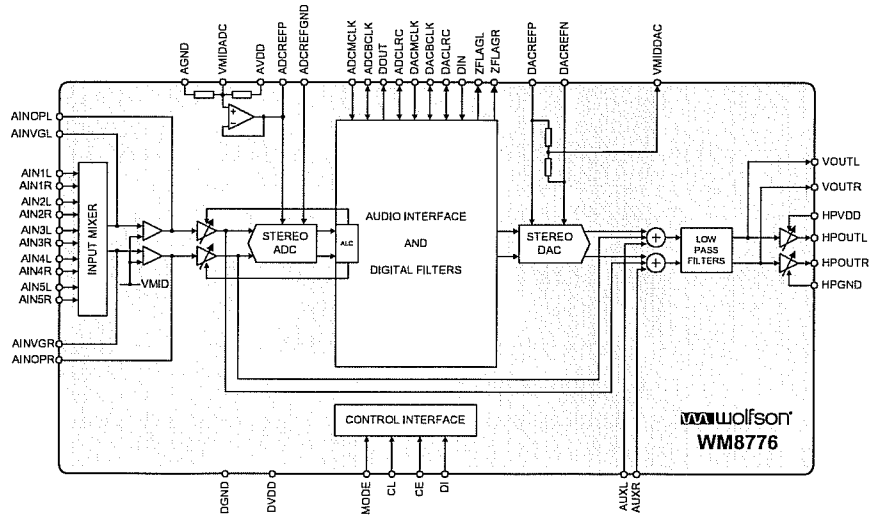
FEATURES

- Audio Performance
  - 108dB SNR ('A' weighted @ 48kHz) DAC
  - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Five stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Programmable Limiter or Automatic Level Control (ALC)
- Stereo DAC with independent analogue and digital volume controls
- Stereo Headphone and Line Output
- 3-Wire SPI Compatible or 2-Wire Software Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- Selectable AUX input to the volume controls
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

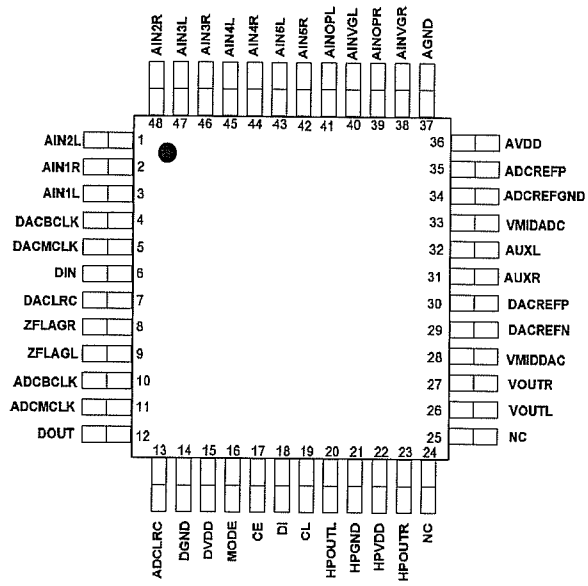
APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8776EFT/V	-25 to +85°C	48-pin TQFP	MSL2	240°C
WM8776EFT/RV	-25 to +85°C	48-pin TQFP (tape and reel)	MSL2	240°C
WM8776SEFT/V	-25 to +85°C	48-pin TQFP (lead free)	MSL2	260°C
WM8776SEFT/RV	-25 to +85°C	48-pin TQFP (lead free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
2	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground
3	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
4	DACBCLK	Digital input/output	DAC audio interface bit clock
5	DACMCLK	Digital input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
6	DIN	Digital Input	DAC data input
7	DACLRC	Digital input/output	DAC left/right word clock
8	ZFLAGR	Open Drain output	DAC Right Zero Flag output (external pull-up resistor required)
9	ZFLAGL	Open Drain output	DAC Left Zero Flag output (external pull-up resistor required)
10	ADCBCLK	Digital input/output	ADC audio interface bit clock
11	ADCMCLK	Digital input	ADC audio interface master clock
12	DOUT	Digital output	ADC data output
13	ADCLRC	Digital input/output	ADC left/right word clock
14	DGND	Supply	Digital negative supply
15	DVDD	Supply	Digital positive supply
16	MODE	Digital input	Control interface mode select (5V tolerant)
17	CE	Digital input	Serial interface Latch signal (5V tolerant)
18	DI	Digital input	Serial interface data (5V tolerant)
19	CL	Digital input	Serial interface clock (5V tolerant)
20	HPOUTL	Analogue Output	Headphone left channel output
21	HPGND	Supply	Headphone negative supply
22	HPVDD	Supply	Headphone positive supply
23	HPOUTR	Analogue Output	Headphone right channel output
24	NC	Not bonded	
25	NC	Not bonded	
26	VOUTL	Analogue output	DAC channel left output
27	VOUTR	Analogue output	DAC channel right output
28	VMIDDAC	Analogue output	DAC midrail decoupling pin ; 10uF external decoupling
29	DACREFN	Analogue input	DAC negative reference input
30	DACREFP	Analogue input	DAC positive reference input
31	AUXR	Analogue input	DAC mixer right channel input
32	AUXL	Analogue input	DAC mixer left channel input
33	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
34	ADCREFGND	Supply	ADC negative supply and substrate connection
35	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
36	AVDD	Supply	Analogue positive supply
37	AGND	Supply	Analogue negative supply and subVstrate connection
38	AINVGR	Analogue Input	Right channel multiplexor virtual ground
39	AINOPR	Analogue Output	Right channel multiplexor output
40	AINVGL	Analogue Input	Left channel multiplexor virtual ground
41	AINOPL	Analogue Output	Left channel multiplexor output
42	AIN5R	Analogue Input	Channel 5 right input multiplexor virtual ground
43	AIN5L	Analogue Input	Channel 5 left input multiplexor virtual ground
44	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
45	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
46	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
47	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
48	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground

Note : Digital input pins have Schmitt trigger input buffers and pins 16, 17, 18 and 19 are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (DI, CL, CE and MODE)	DGND -0.3V	+7V
Voltage range digital inputs (MCLK, DIN, ADCLRC, DACLRC, ADCBCLK and DACBCLK)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, HPVDD, DACREFP		2.7		5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}=1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
DAC Performance (Load = 10k Ω, 50pF)						
0dBFs Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, @ fs = 48kHz		108		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input		108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Headphone Buffer						
Maximum Output voltage				0.9		Vrms
Max Output Power (Note 4)	P_o	R_L = 32 Ω		25		mW
		R_L = 16 Ω		50		mW
SNR (Note 1,2)		A-weighted	85	92		dB
Headphone analogue Volume Gain Step Size			0.5	1	1.5	dB
Headphone analogue Volume Gain Range		1kHz Input	-73		+6	dB
Headphone analogue Volume Mute Attenuation		1kHz Input, 0dB gain		100		dB
Total Harmonic Distortion +Noise	THD+N	1kHz, R_L = 32Ω @ P_o = 10mW rms		-80 0.01	-60 0.1	dB %
		1kHz, R_L = 32Ω @ P_o = 20mW rms		-77 0.014	-40 1.0	dB %
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz, without supply decoupling		-40		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz		102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz 64 x OSR		100		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-90	-80	DB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

		1kHz, -3dBFs		-95	-85	dB
ADC Channel Separation		1kHz Input		90		dB
Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Mute Attenuation (Note 6)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Analogue input (AIN) to Analogue output (VOUT) (Load=10k Ω, 50pF, gain = 0dB) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1)			90	100		dB
THD		1kHz, 0dB		-90		dB
		1kHz, -3dB		-95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Mute Attenuation		1kHz, 0dB		100		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		8		mA

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. Harmonic distortion on the headphone output decreases with output power.
5. All performance measurement done using certain timings conditions (Please refer to section 'Digital Audio Interface').
6. A better MUTE Attenuation can be achieved if the ADC gain is set to minimum.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

TFT LCD Approval Specification

MODEL NO.: V420H1 - L05

- CONTENTS –

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H1-L05 is a 42” TFT Liquid Crystal Display module with 20-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (1200:1)
- Fast response time (Gray to gray average 6.5ms)
- High color saturation (NTSC 75%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 50/60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

×	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02” diagonal)	mm	(1)
Bezel Opening Area	938.3 (H) x 531.3 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 25%) Hard coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	982.3	983.0	984.0	mm	(1), (2)
	Vertical (V)	575.3	576.0	577.0	mm	
	Depth (D)	51.3	52.3	53.3	mm	
Weight		13100	13300	13500	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	(50)	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

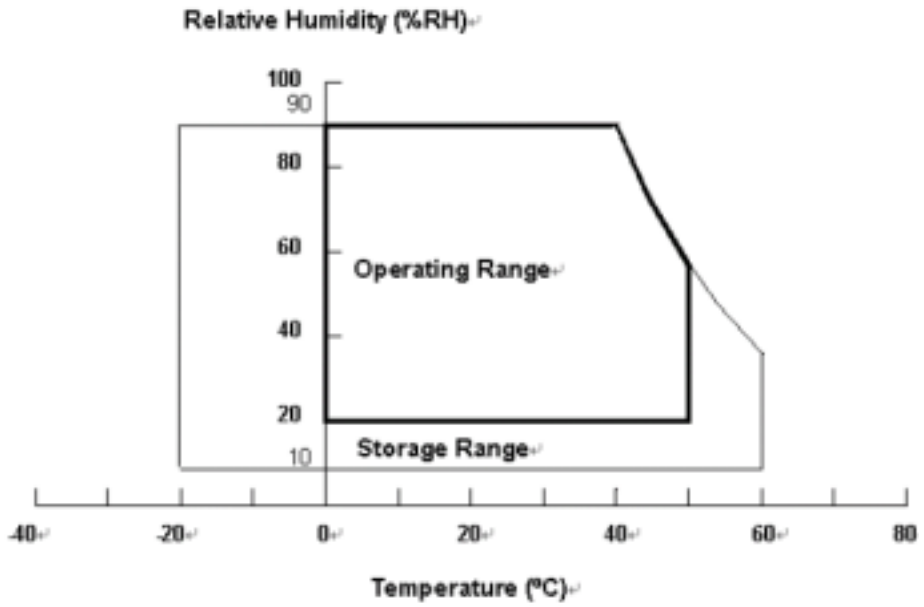
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	20	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

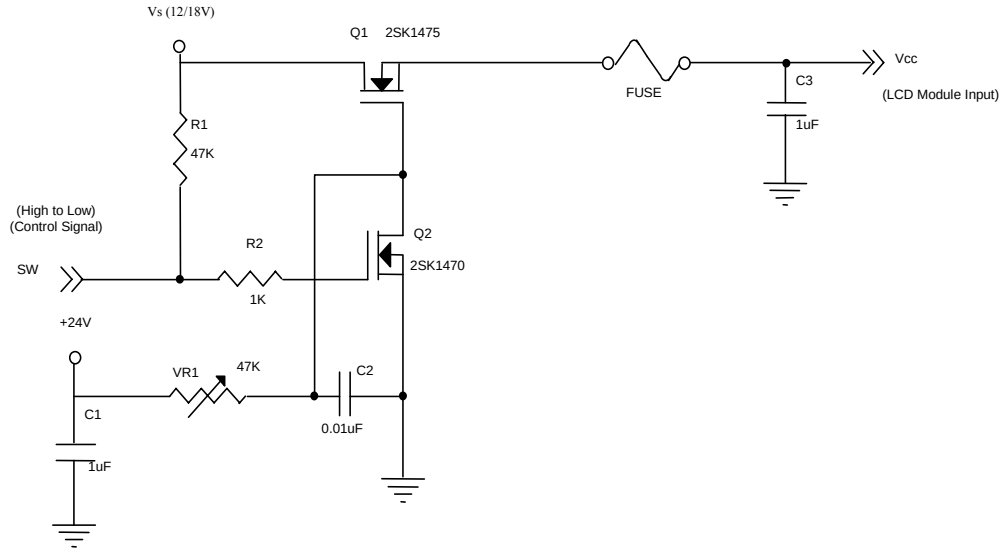
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE (Ta = 25 ± 2 ºC)

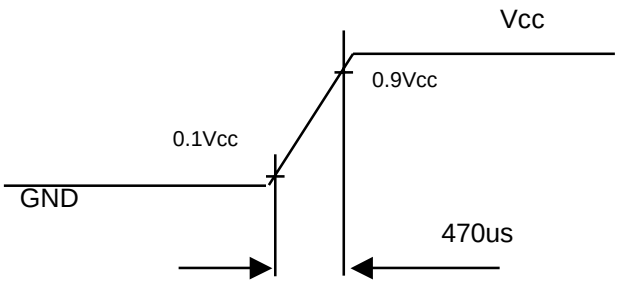
Parameter			Symbol	Value			Unit	Note
				Min.	Typ.	Max.		
Power Supply Voltage			V_{CC}	10.8	12	13.2	V	(1)
				16.2	18	19.8		
Power Supply Ripple Voltage			V_{RP}	-	-	350	mV	
Rush Current			I_{RUSH}	2.5	-	3.5	A	(2)
Power Supply Current		White	I_{CC}	-	0.80	1.0	A	(3)
		Black		-	0.35	-	A	
		Vertical Stripe		-	0.62	-	A	
		White	I_{CC}	-	1.20	1.5	A	(4)
		Black		-	0.50	-	A	
		Vertical Stripe		-	0.90	-	A	
LVDS Interface	Differential Input High Threshold Voltage		V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage		V_{LVTL}	-100	-	-	mV	
	Common Input Voltage		V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor		R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage		V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage		V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

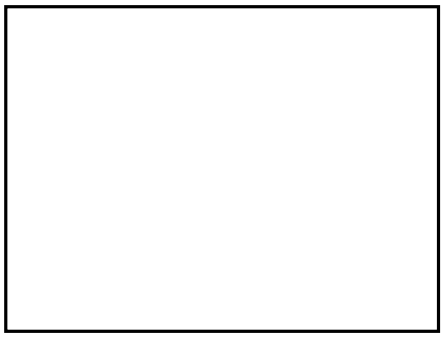


Vcc rising time is 470us



Note (3)&(4) The specified power supply current is under the conditions at Vcc = 18 V(Note(3)), Vcc = 12V(Note(4)), Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

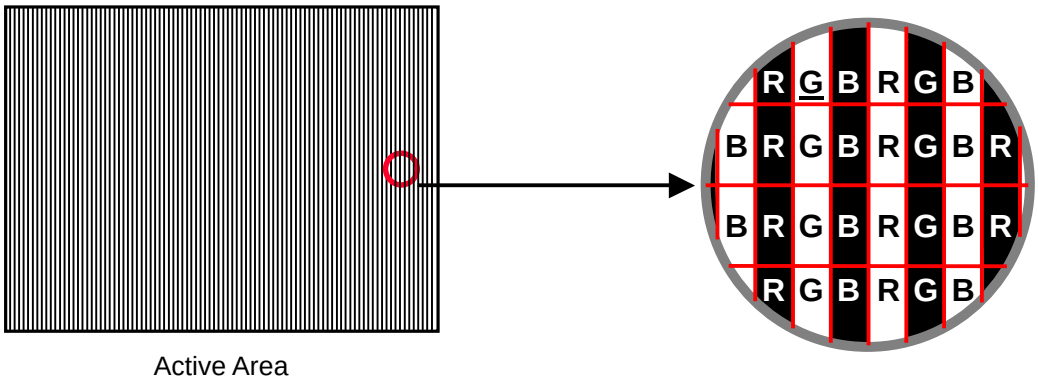


Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1300	-	V_{RMS}	-
Lamp Current	I_L	6.0	6.5	7.0	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	2200	V_{RMS}	(2), Ta = 0 ºC
		-	-	2000	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	182	192	W	(5)(6), I_L = 6.5mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	7.6	8.0	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL}=22.8V
Backlight Turn on Voltage	V_{BS}	2200	-	-	V_{RMS}	Ta = 0 ºC
		2000	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	47	50	53	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

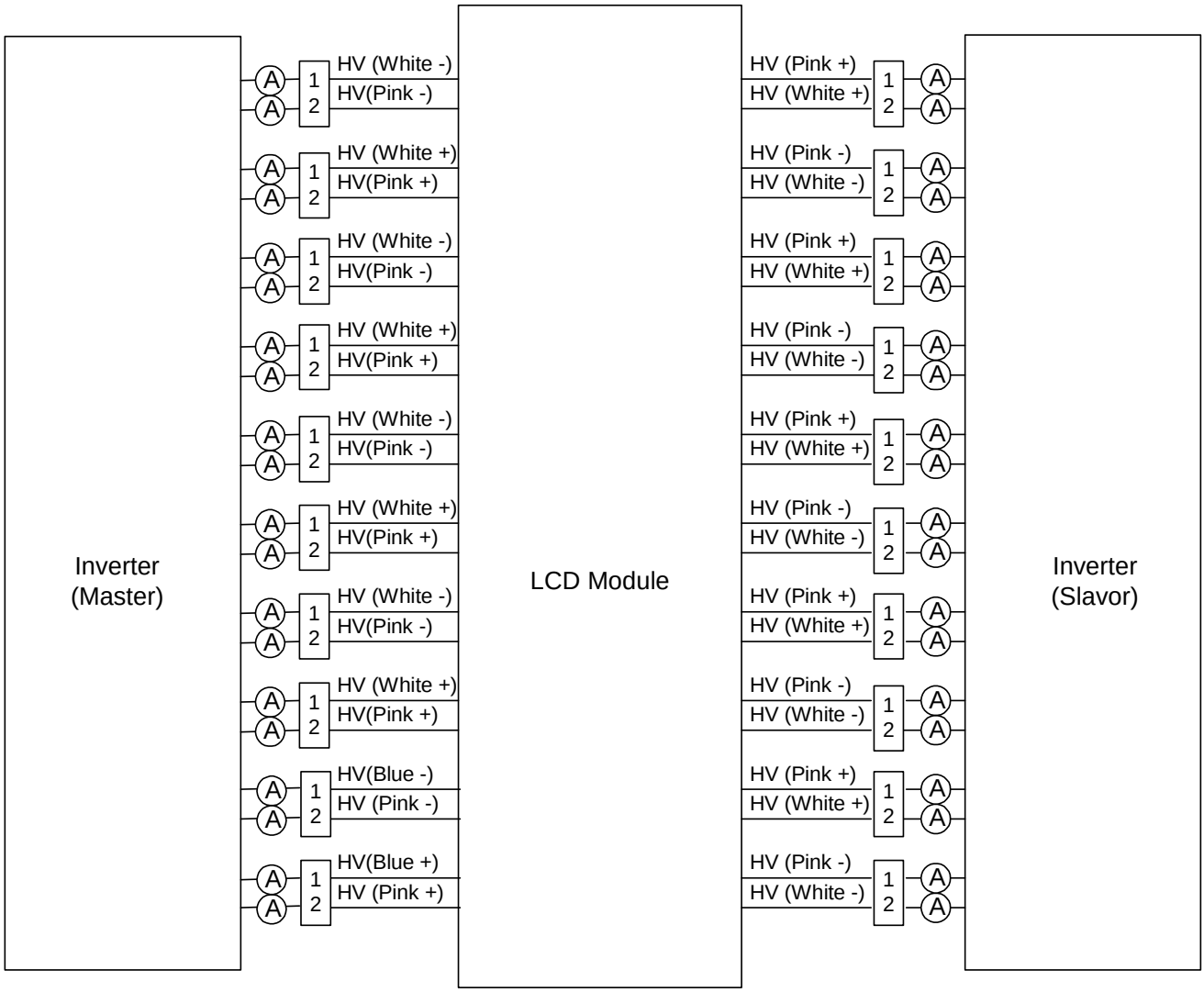
Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 6.0~ 7.0mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 42" backlight unit under input voltage 24V, average lamp current 6.8 mA and lighting 30 minutes later.


Inverter
(Master)
HV (White -)
HV(Pink -)
HV (White +)
HV(Pink +)
HV (White -)
HV(Pink -)
HV (White +)
HV(Pink +)
HV (White -)
HV(Pink -)
HV (White +)
HV(Pink +)
HV (White -)
HV(Pink -)
HV (White +)
HV(Pink +)
HV(Blue -)
HV (Pink -)
HV(Blue +)
HV (Pink +)
LCD Module
HV (Pink +)
HV (White +)
HV (Pink -)
HV (White -)
HV (Pink +)
HV (White +)
HV (Pink -)
HV (White -)
HV (Pink +)
HV (White +)
HV (Pink -)
HV (White -)
HV (Pink +)
HV (White +)
HV (Pink -)
HV (White -)
HV (Pink +)
HV (White +)
HV (Pink -)
HV (White -)
Inverter
(Slavor)

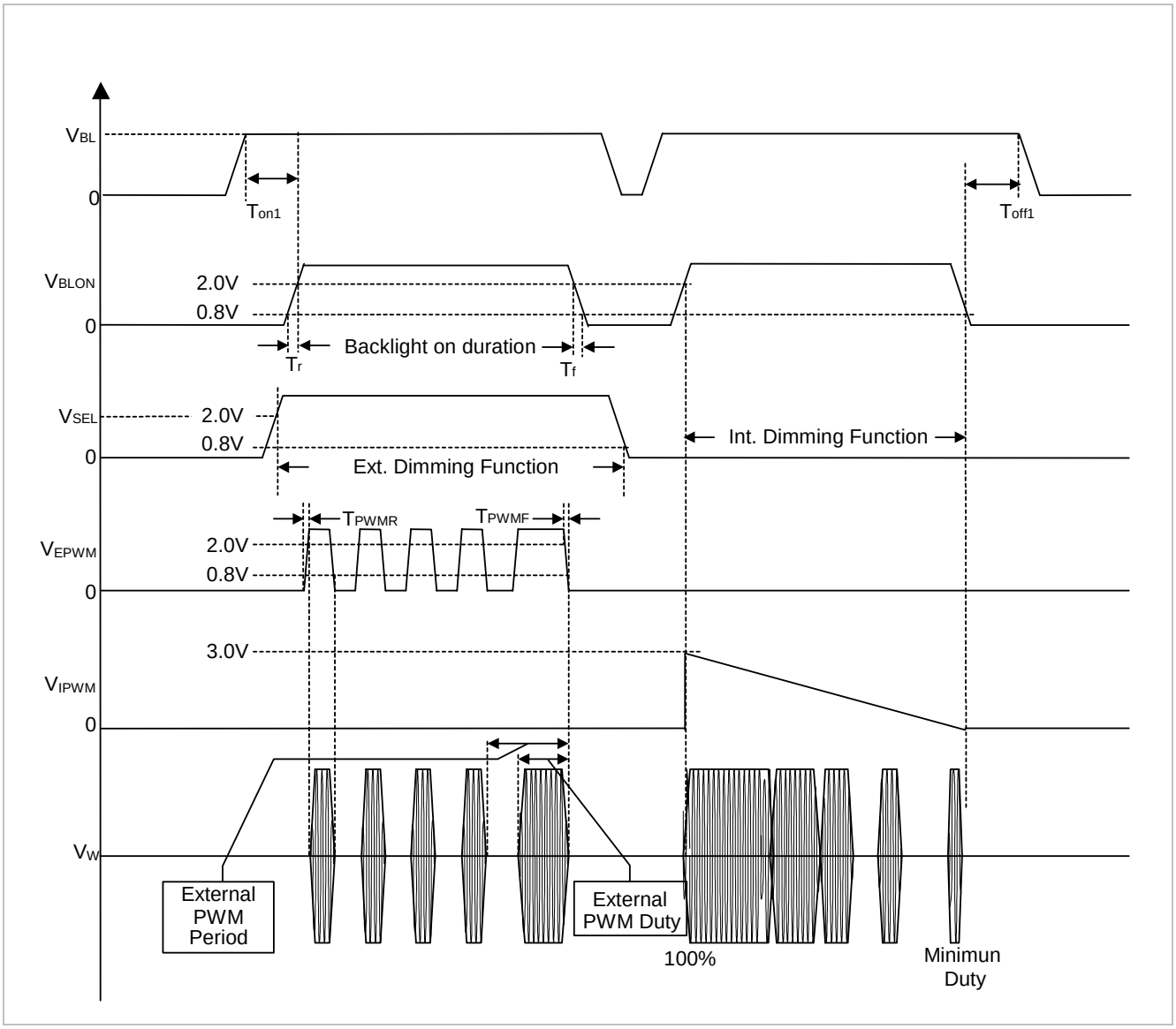
3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—-	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	1	—	—	ms	
BLON Off Time		T_{off}	—	1	—	—	ms	

Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

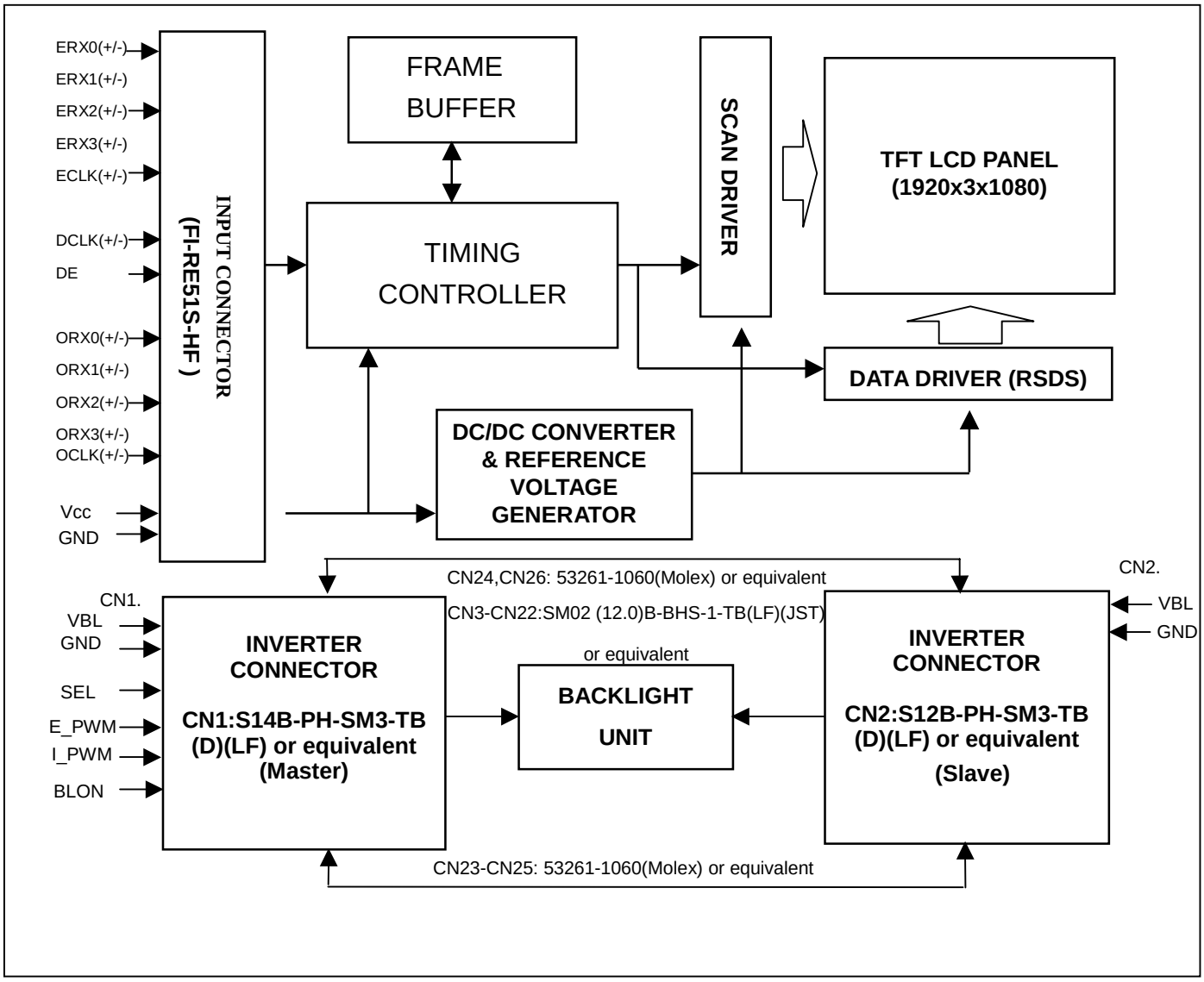
Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.


VBL
0
Ton1
Toff1
VBLON
2.0V
0.8V
0
Tr
Backlight on duration
Tf
VSEL
2.0V
0.8V
0
Int. Dimming Function
Ext. Dimming Function
TPWMR
TPWMF
VEPWM
2.0V
0.8V
0
3.0V
VIPWM
0
VW
External PWM Period
External PWM Duty
100%
Minimun Duty

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

Connector part no. : FI-RE51S-HF (JAE) or equivalent.

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(3)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	NC	No Connection	
8	RPF	Display Rotation	(1)
9	ODSEL	Overdrive Lookup Table Selection	(2)
10	NC	No Connection	(3)
11	GND	Ground	
12	ORX0-	Odd pixel, Negative LVDS differential data input. Channel 0	
13	ORX0+	Odd pixel, Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel, Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel, Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel, Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel, Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel, Negative LVDS differential clock input.	
20	OCLK+	Odd pixel, Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Odd pixel, Negative LVDS differential data input. Channel 3	
23	ORX3+	Odd pixel, Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(3)
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ERX0-	Even pixel, Negative LVDS differential data input. Channel 0	
29	ERX0+	Even pixel, Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel, Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel, Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel, Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel, Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel, Negative LVDS differential clock input.	
36	ECLK+	Even pixel, Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel, Negative LVDS differential data input. Channel 3	
39	ERX3+	Even pixel, Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(3)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	

47	GND	Ground	
48	VCC	Power input (+12V or +18.0V)	
49	VCC	Power input (+12V or +18.0V)	
50	VCC	Power input (+12V or +18.0V)	
51	VCC	Power input (+12V or +18.0V)	

Note (1) Low : normal display (default), High : display with 180 degree rotation

Note (2) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (3) Reserved for interval use. Left it open.

5.2 BACKLIGHT UNIT

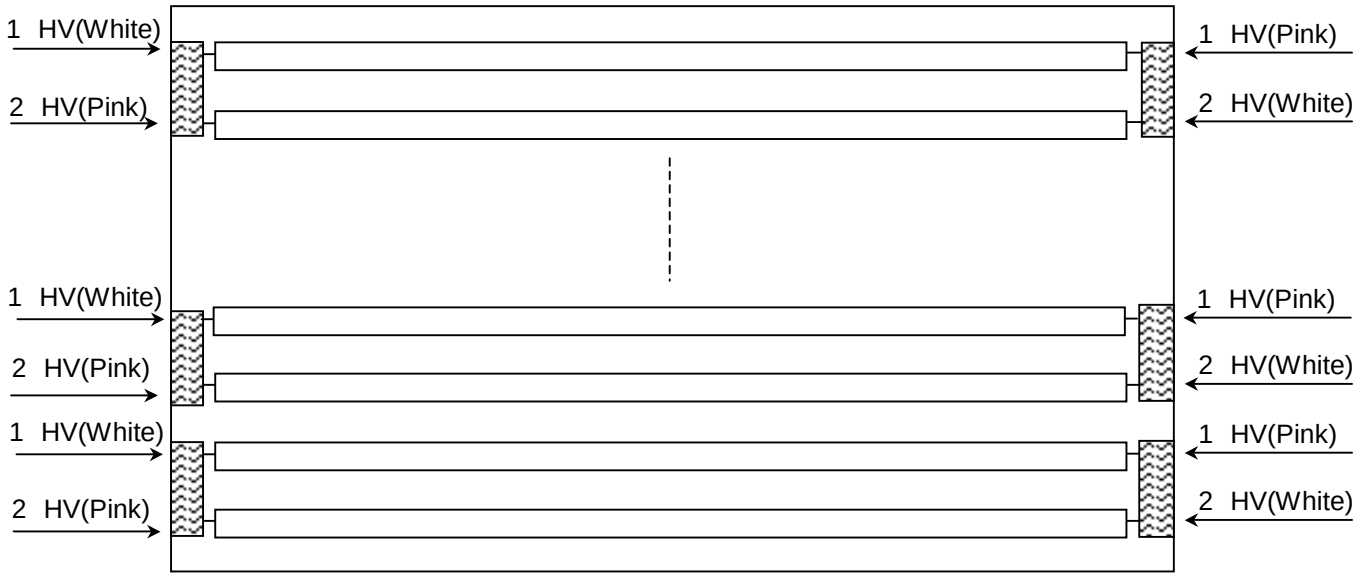
The pin configuration for the housing and the leader wire is shown in the table below.

CN3-CN22: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST.

The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).



5.3 INVERTER UNIT

CN1 (Header): S14B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	$+24V_{DC}$ power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
12	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = Low).
13	I_PWM	Internal PWM Control Signal I_PWM should be connected to ground when external PWM was selected (SEL = High).
14	BLON	Backlight on/off control

CN2 (Header): S12B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	$+24V_{DC}$ power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3- CN22 (Header): SM02(12.0)B-BHS-1-TB (LF)(JST) or equivalent

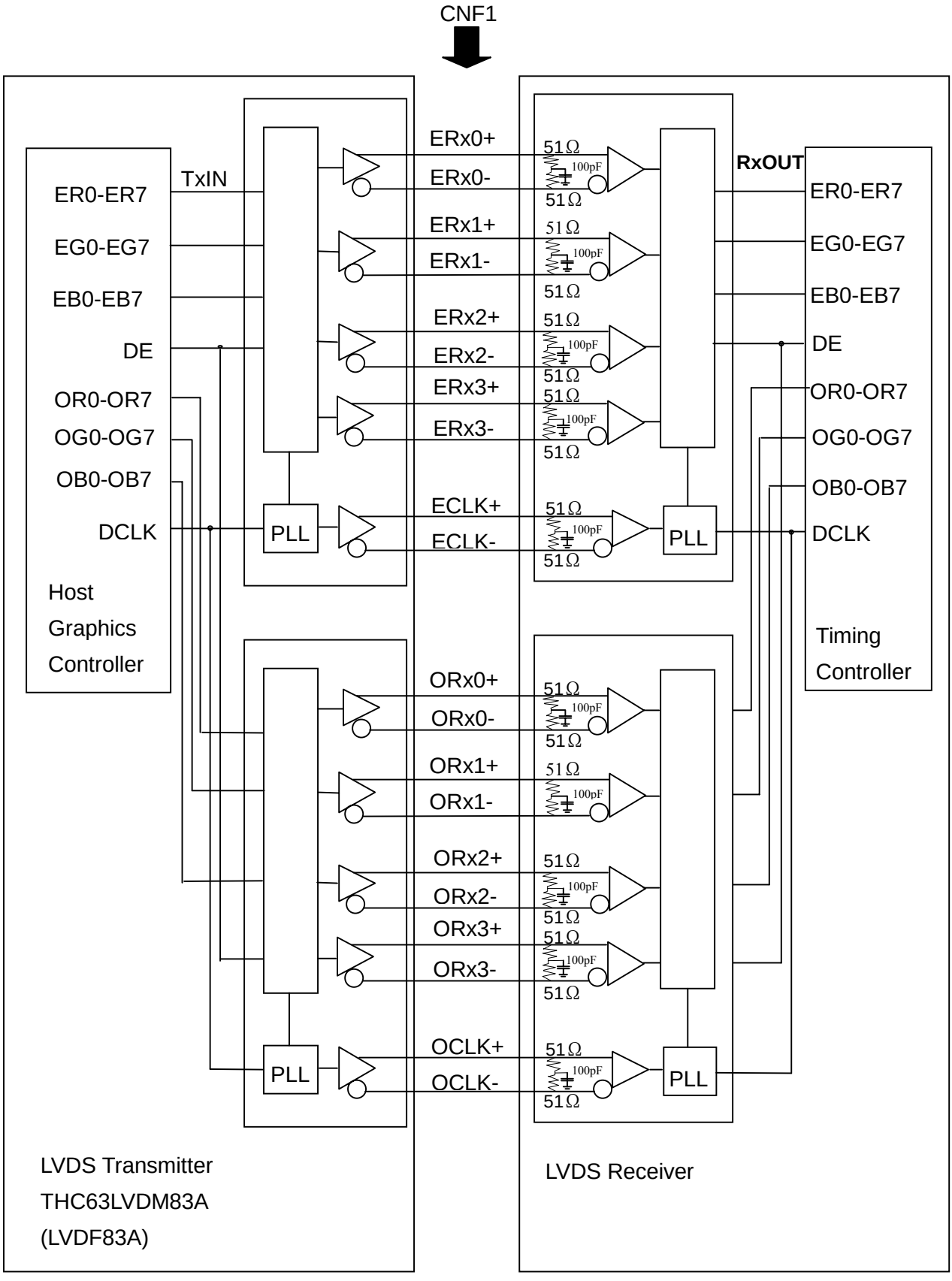
Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN23-CN26 (Header): 53261-1060(Molex) or equivalent

Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Notes: (1) The system must have the transmitter to drive the module.
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
(3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.5 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2			30	Rx OUT2	R2
	R3	55	TxIN3			32	Rx OUT3	R3
	R4	56	TxIN4	TA OUT0-	Rx 0-	33	Rx OUT4	R4
	R5	3	TxIN6			35	Rx OUT6	R5
	G0	4	TxIN7			37	Rx OUT7	G0
	G1	6	TxIN8			38	Rx OUT8	G1
	G2	7	TxIN9			39	Rx OUT9	G2
	G3	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3
	G4	12	TxIN13			45	Rx OUT13	G4
	G5	14	TxIN14			46	Rx OUT14	G5
	B0	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0
	B1	19	TxIN18			51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20			54	Rx OUT20	B3
	B4	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26			6	Rx OUT26	DE
	R6	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6
	R7	2	TxIN5			34	Rx OUT5	R7
	G6	8	TxIN10			41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
	RSVD 1	25	TxIN23			2	Rx OUT23	Not connect
	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	Not connect
	RSVD 3	28	TxIN25			5	Rx OUT25	Not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

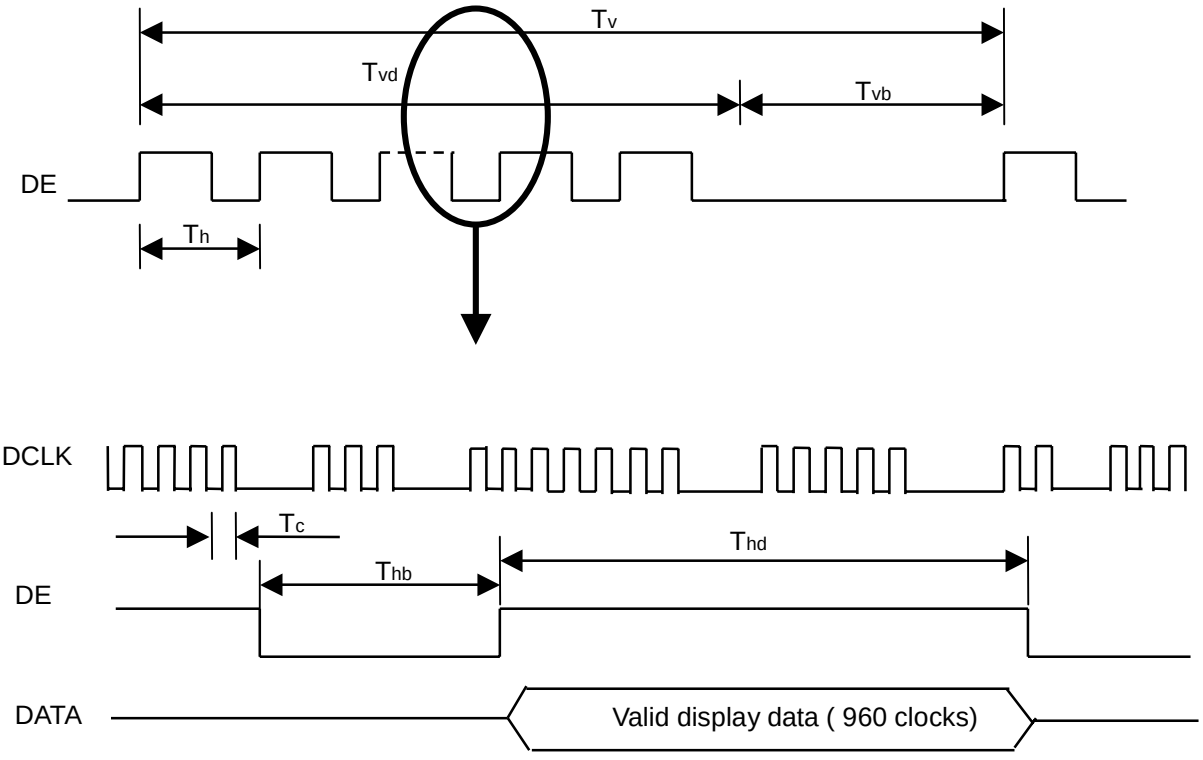
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	(60)	74	(80)	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(1)
		Fr6	57	60	63	Hz	(2)
	Total	Tv	(1115)	1125	(1139)	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	(35)	45	(59)	Th	-
Horizontal Active Display Term	Total	Th	(2100)	2200	(2300)	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
	Blank	Thb	(180)	280	(380)	Tc	-

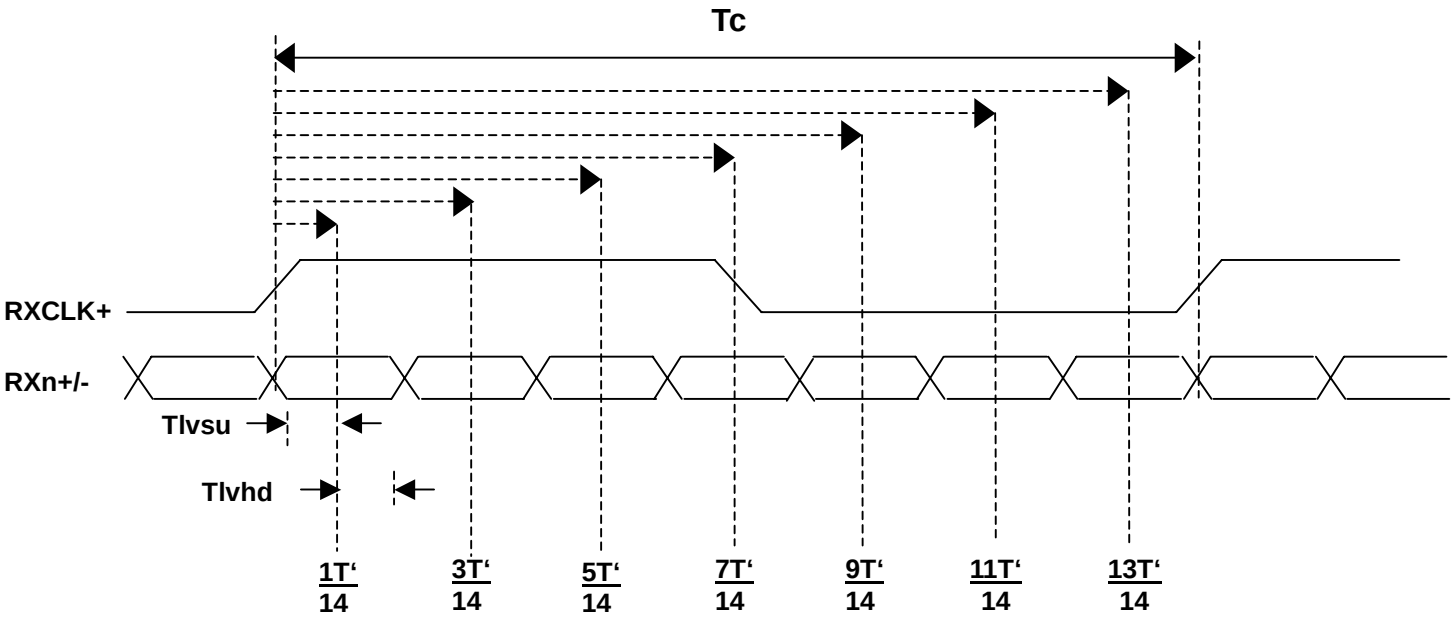
Note (1) (ODSEL) = (H). Please refer to 5.1 for detail information.

(2) (ODSEL) = (L). Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

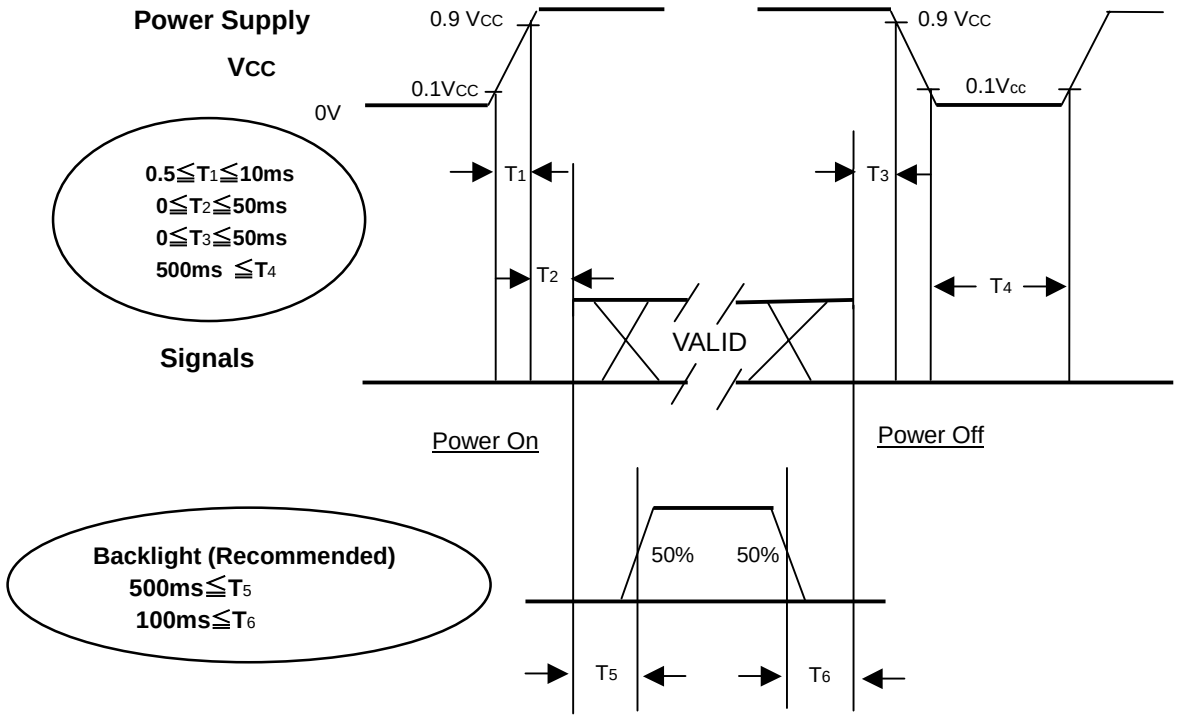


LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen. There is no reliability issue when the T5, T6 timing missing the range.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12/18	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		

Lamp Current	I_L	6.5±0.5	mA
Oscillating Frequency (Inverter)	F_W	50±3	KHz
Vertical Frame Rate	Fr	60	Hz

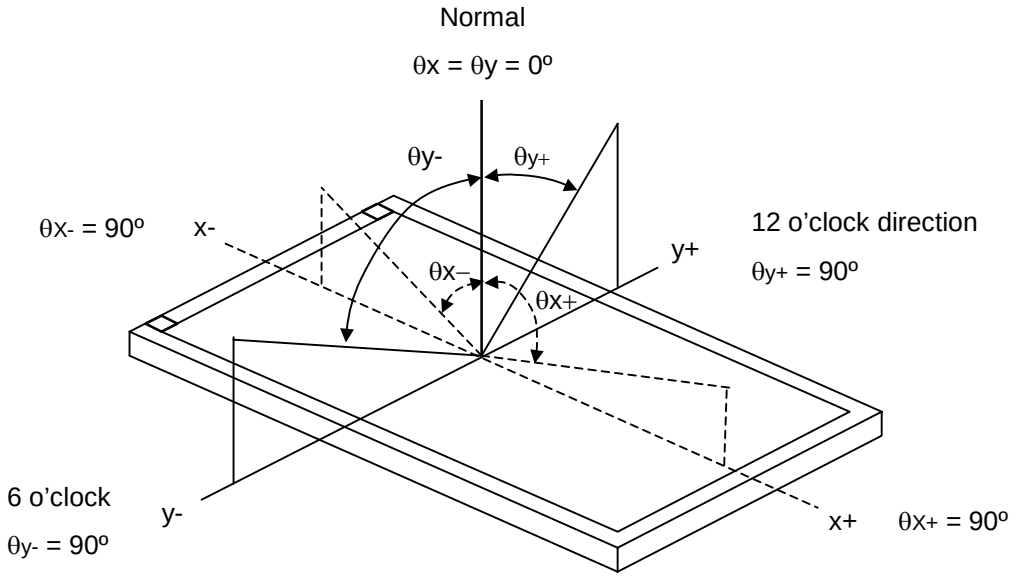
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	900	1200		-	Note (2)
Response Time		Gray to gray			6.5	12	ms	Note (3)
Center Luminance of White		L_C		400	500		cd/m^2	Note (4)
White Variation		δW				1.3	-	Note (7)
Cross Talk		CT				4	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.651	Typ. +0.03	-	Note (6)
		Ry			0.330		-	
	Green	Gx			0.274		-	
		Gy			0.596		-	
	Blue	Bx			0.142		-	
		By			0.067		-	
	White	Wx			0.285		-	
		Wy			0.293		-	
	Color Gamut			72	75		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88		Deg.	Note (1)
		θ_x-		80	88			
	Vertical	θ_Y+		80	88			
		θ_Y-		80	88			

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

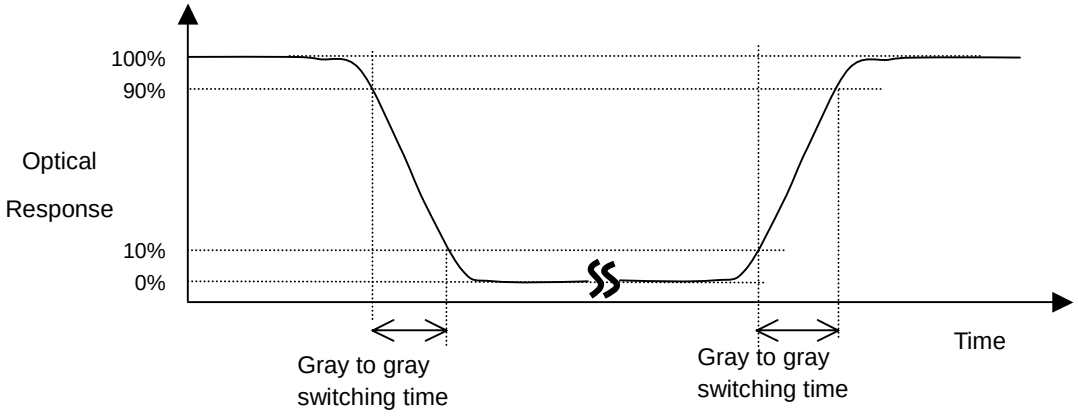
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0, 63,127,191,255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (7).

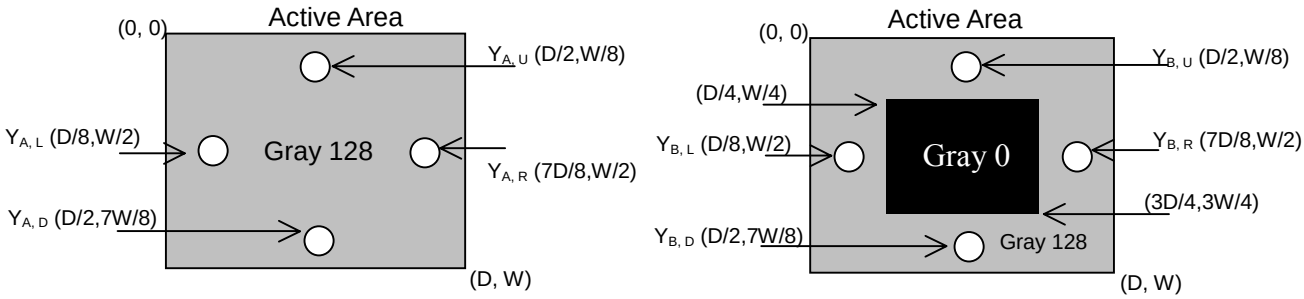
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

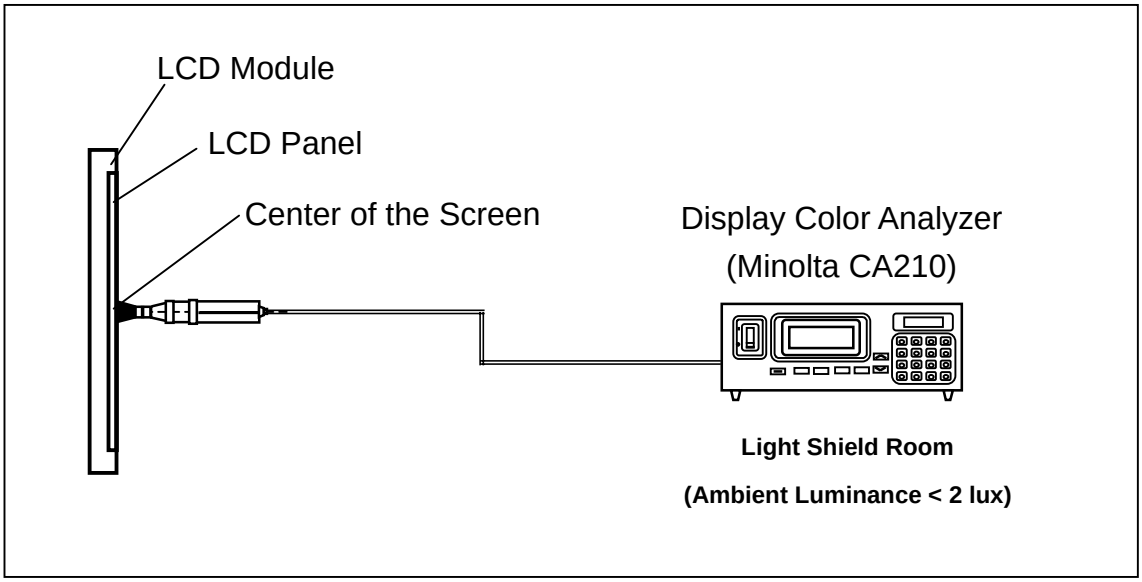
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

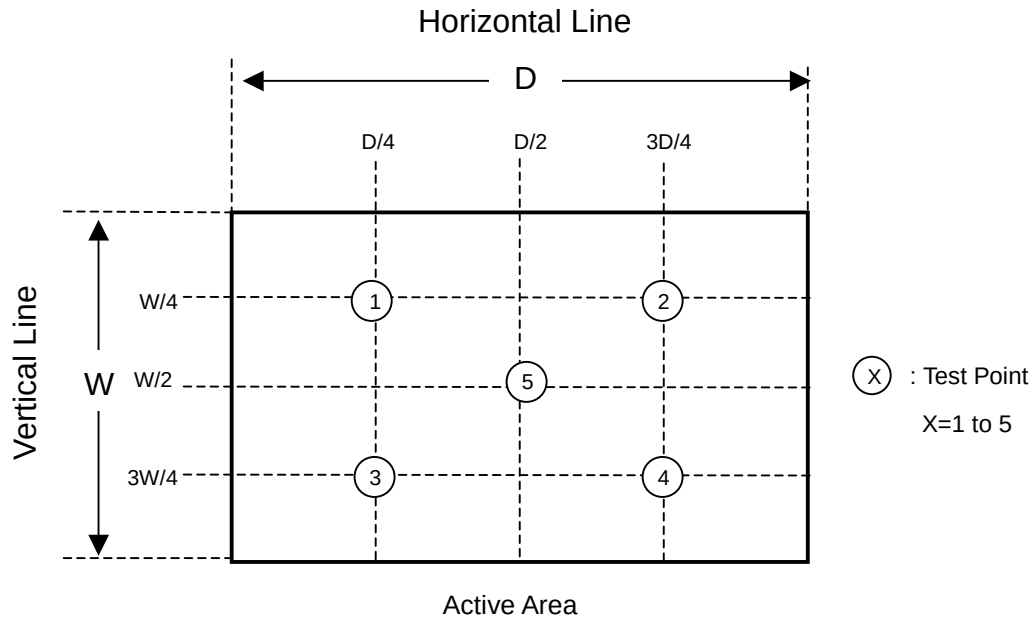
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

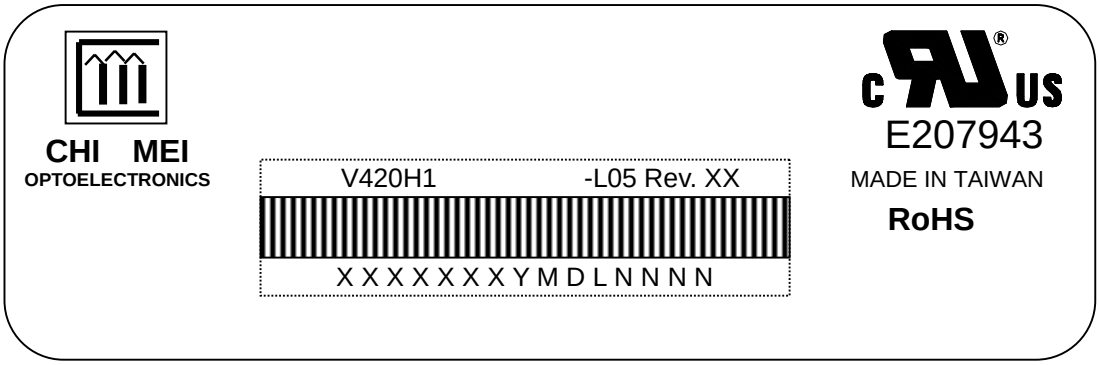
(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

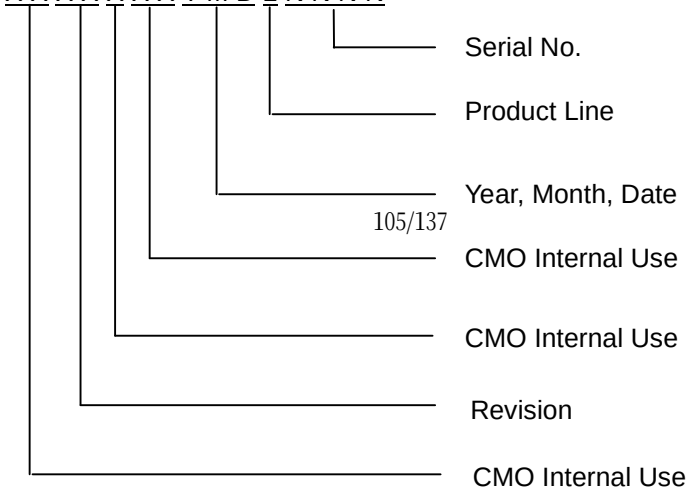
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V420H1-L05

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKONG SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1086(L) X 356 (W) X 715 (H)

(3) Weight : approximately 46.5Kg (3 modules per box)

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

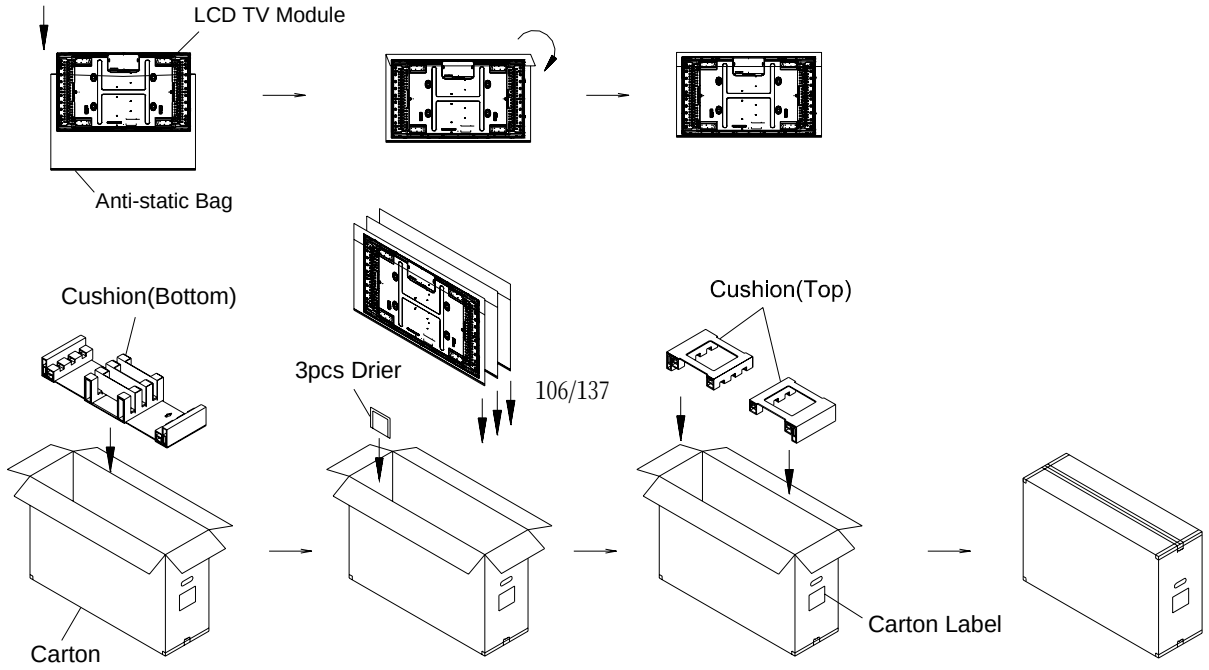


Figure.10-1 packing method

Corner Protector:L1400*50mm*50mm
L1000*50mm*50mm
Pallet:L1100*W1100*H140mm
Pallet Stack:L1100*W1100*H1575mm
Gross:294kg

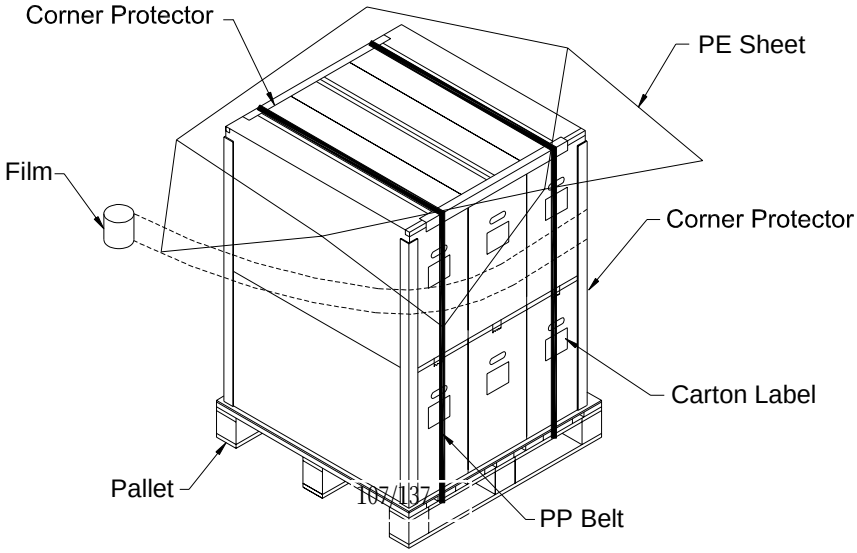
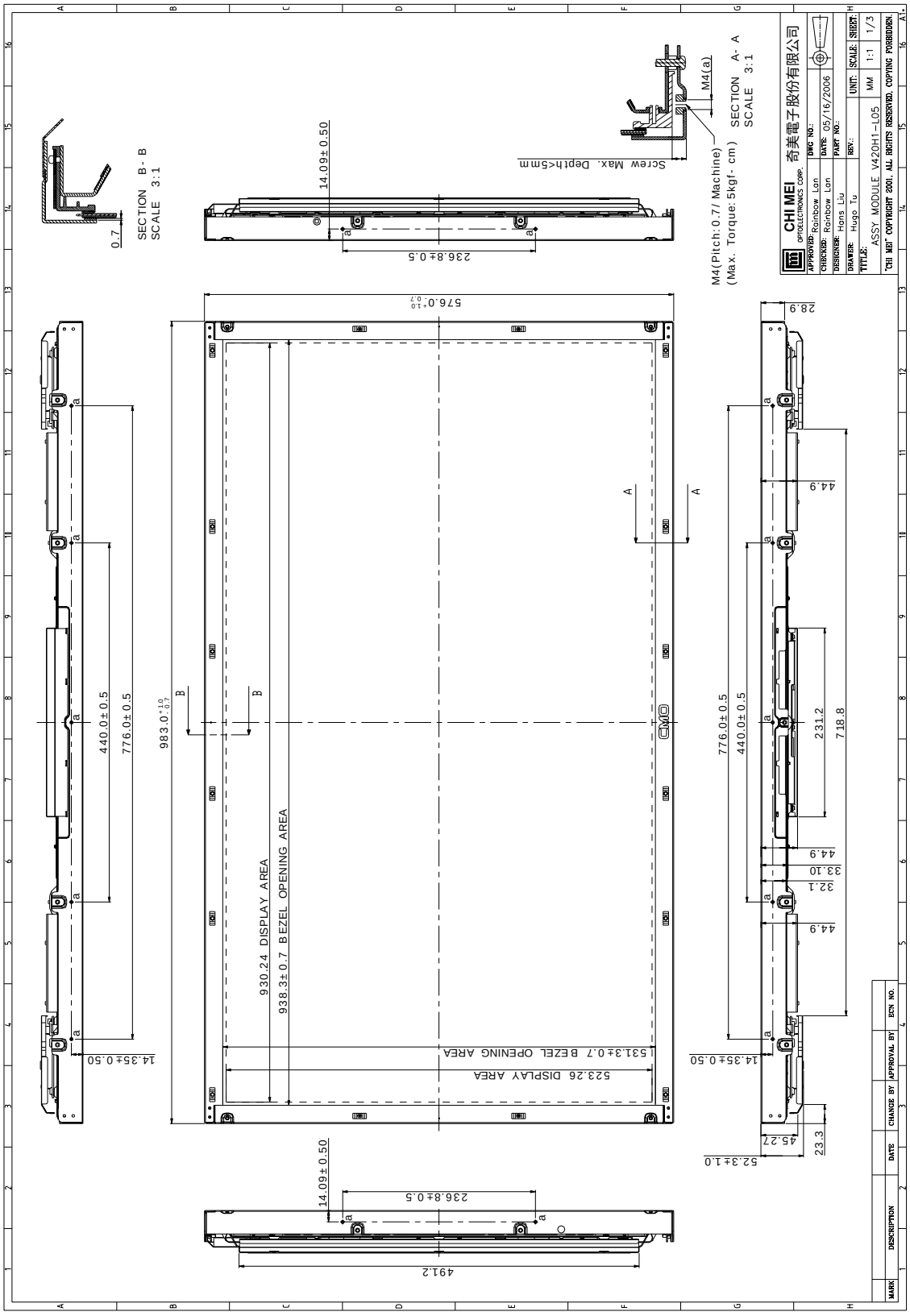
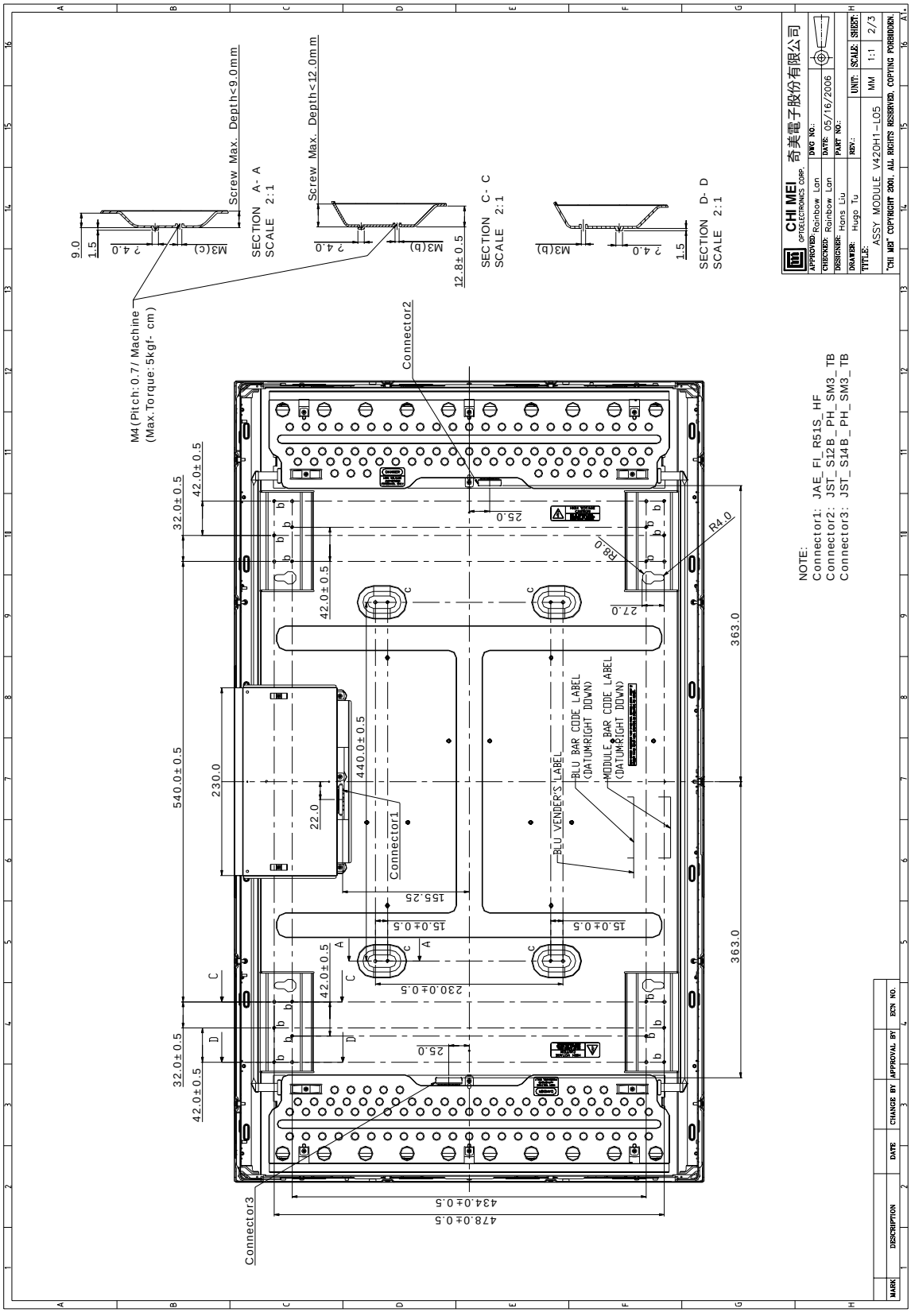
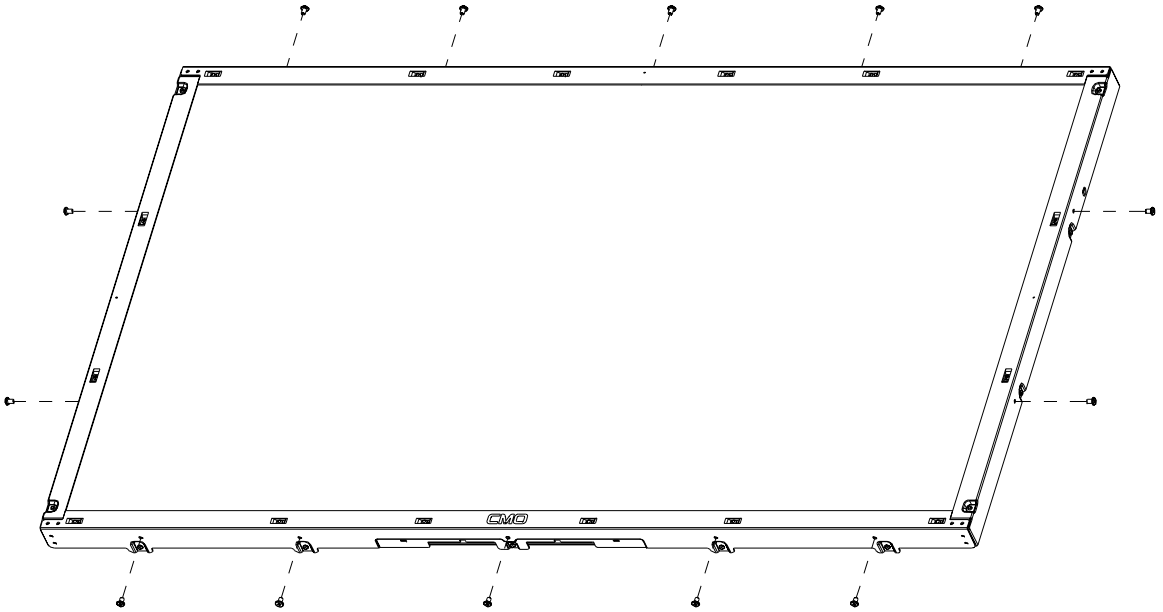


Figure.10-2 Packing method

11. MECHANICAL CHARACTERISTICS




CHI MEI 奇美電子股份有限公司
OPTOELECTRONICS CORP.
APPROVED: Rainbow Lan
CHECKED: Rainbow Lan
DESIGNER: Hans Liu
DRAWER: Hugo Tu
TITLE: ASSY MODULE V420H1-L05
DWG NO.:
DATE: 05/16/2006
PART NO.:
REV.:
UNIT: MM
SCALE: 1:1
SHEET: 2/3
"CHI MEI" COPYRIGHT 2001, ALL RIGHTS RESERVED. COPYING FORBIDDEN.
NOTE:
Connector1: JAE_FI_R51S_HF
Connector2: JST_S12B_PH_SM3_TB
Connector3: JST_S14B_PH_SM3_TB
Screw Max. Depth<9.0mm
Screw Max. Depth<12.0mm
M4(Pitch:0.7/ Machine
(Max.Torque:5kgf- cm)
SECTION A- A
SCALE 2:1
SECTION C- C
SCALE 2:1
SECTION D- D
SCALE 2:1
Connector1
Connector2
Connector3
BLU VENDER'S LABEL
BLU BAR CODE LABEL
(DATUM:RIGHT DOWN)
MODULE BAR CODE LABEL
(DATUM:RIGHT DOWN)
540.0±0.5
478.0±0.5
434.0±0.5
363.0
230.0±0.5
155.25
440.0±0.5
230.0
22.0
42.0±0.5
32.0±0.5
25.0
27.0
R4.0
R8.0
MARK
DESCRIPTION
DATE
CHANGE BY
APPROVAL BY
ECN NO.



Note:
1. It is recommended that all screws should be included when CMO's product is applied in order to guarantee structure strength of product.
2. Screw: M4(Pitch 0.7 / Machine)
3. Torque: 4~5kgf.cm

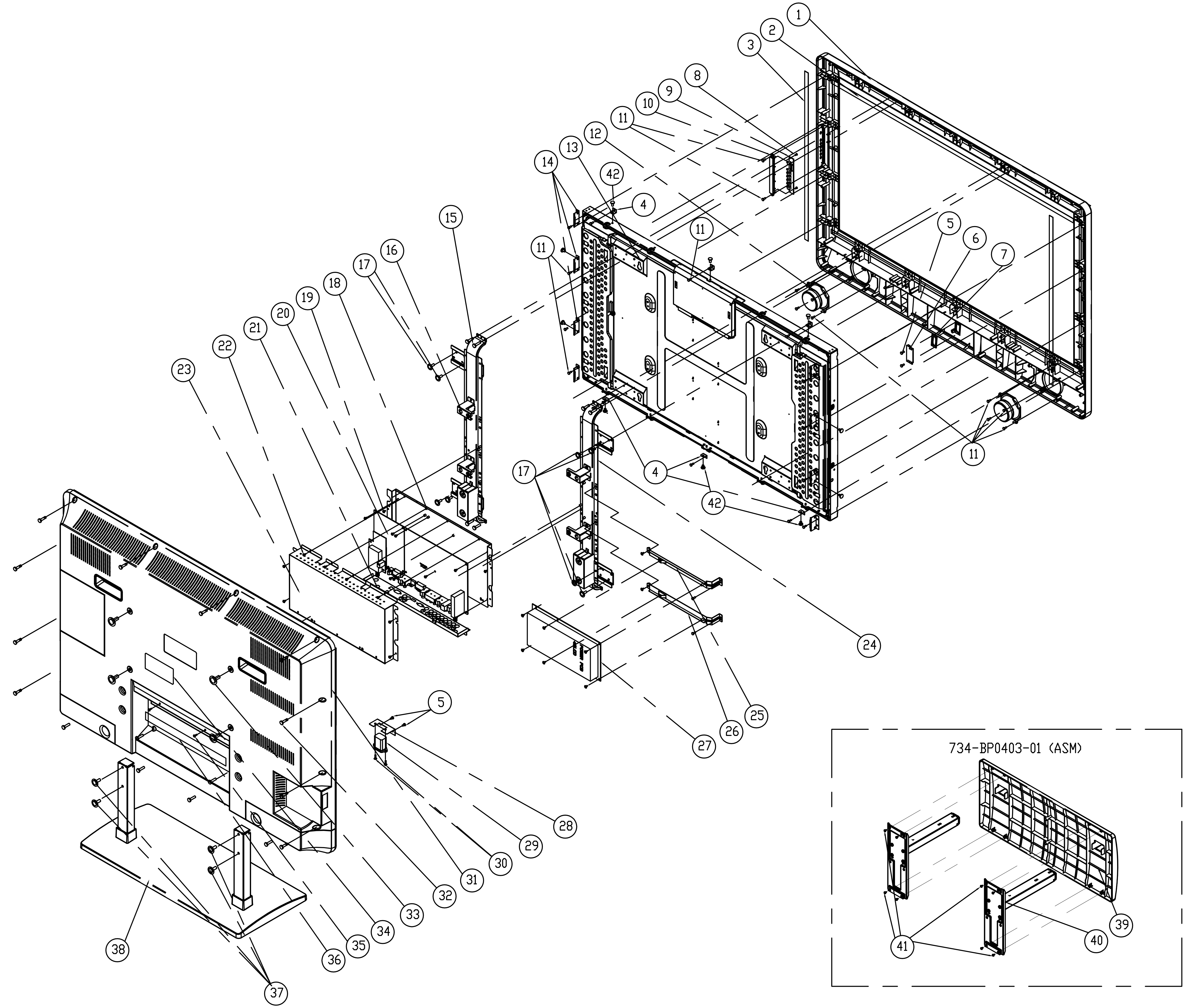
MARK	DESCRIPTION	DATE	CHANGE BY	APPROVAL BY	ECN NO.

CHI MEI OPTOELECTRONICS CORP. 奇美電子股份有限公司					
APPROVED: Rainbow Lan	DWG NO.:				
CHECKED: Rainbow Lan	DATE: 05/16/2006				
DESIGNER: Hans Liu	PART NO.:				
DRAWER: Hugo Tu	REV.:	UNIT:	SCALE:	SHEET:	
TITLE: ASSY MODULE V420H1-L05		MM	1:1	3/3	

A1

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY

DWG. REV.	ZONE	DESCRIPTION	DATE	REVISOR



ITEM	PART NO.	DESCRIPTION	QTY	REMARK
45				
44				
43				
42	604-407005-10	MACH. SCREW BINDING HEAD M5X0.8PX15MM	10	
41	612-300108-00	S-TAP.SCREW WHR 3X8	8	
40	712-BP0402-01	STAND SUPPORT ASSY BP04 H=270MM BLACK	2	ASM
39	231-BP0401-02AR	BASE COVER BP04 MATT BLACK	1	
38	734-BP0403-02	PLASTIC STAND FOR 42LD CD=460MM W/PACKING EXPLODE H=270MM MATT B	1	ASM
37	60D-508015-00	MACH SCREW W/SPRING WASHER M5X0.8X15MM BLACK ZN PLATE	4	
36	578-L37AD01-01AP	FUNCTION SHEET FOR TERMINAL LCT37" S-MT8202 USA P	1	
35	602-305008-00	MACH SCREW PAN-WASHER M3X8 BZNP+H	4	
34	560-L42AE01-02AP	MODEL LABLE AKAI LCT4226TA S-MT8206 USA P	1	
33	602-601010-00	MACH SCREW PAN WASHER M6.0X1.0PX10MM BLACK Zn PLATED	4	
32	614-400412-00	S-TAP.SCREW BID 4X12	26	
31	202-L42AE03-01AA	CABINET BACK BLACK W/O DVD/POWER SWITCH LCT4226TH	1	
30	601-305008-00	MACH.SCREW CTS 3X8 BZN +H	2	
29	E3421-925118	WIRE ASSY 8P2.5/7P2.0 L170MM 5V 12V SIGNAL POWER MT8202	1	
28	426-L37AD02-01S	AC JACK BRACKET	1	
27	E7801-P02004	POWER SWITCH	1	
26	G429-L42AE02-01SA	PCB ASSY PSU BOARD MEGMEET MLT198L FOR 42"LCD	1	
25	G429-L42AE01-01SA	ROHS POWER BKT TOP	1	
24	713-L42AE02-01	MAIN BKT ASSY LEFT	1	ASM
23	483-L32AB32-01S	SHIELDING COVER	1	
22	602-305004-10	MACH. SCREW PAN-WASHER M3X4 NIP +H	8	
21	436-L32AB0G-01S	TERMINAL SHEET FOR COMPONENT X2	1	
20	E3761-058010-6	PCB V0 250X175 MAIN MT8202 4LA YER	1	
19	602-305006-10	MACH.SCREW WHR 3X6	24	
18	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1	
17	60D-407008-10	MACHSCREW W/SPRING WASHER M4X0.7PX8MM ZNP	8	
16	713-L42AE01-01	MAIN BKT ASSY RGHT	1	ASM
15	614-400412-00	S-TAP.SCREW BID 4X12	26	
14	G429-L42AE08-01SA	ROHS BKT FOR CMO SIDE	8	
13	E6203-42PD01	DISPLAY LCD 42" LPL WUXGA TFT LC420WU1-SLA2	1	
12	E4801-124001	SPEAKER 8 OHM 10W D3" YD78-1	2	
11	614-300110-10	S-TAP.SCREW BID 3X10	30	
10	277-l37AE01-02AS	FUNCTION KNOB SILVER S	1	
9	E3701-065010	PCB V0 KEY SINGLE(120X17MM) 8 IN 1(140X136MM) FOR LCT42AE	1	
8	610-260208-10	S-TAP.SCREW RND 2.6X8	2	
7	459-L32AD01-01	SHORT 'L' BKT FOR PANEL L37AD	1	
6	E3701-051060	PCB V0 REMOTE 54X25 FOR 32LCD TV+DVD TV FUNCTION	1	
5	614-300107-00	SELF TAPPING SCREW BINDING HEAD 3.0X7.0	4	
4	429-L37AD02-01	SHORT 'L' BKT FOR PANEL	6.	
3	521-550155-01	FELT PAPER 550X15X0.5MM W/ADHESIVE	2	
2	521-95015-01	FELT PAPER 950X15X0.5MM W/ADHESIVE	2	
1	200-L42AE01-01AA	CABINET FRONT MATT BLACK/SILVER	1	

DRAWN.					
CHECKED					
APPRD.					
3rd ANGLE PROJECTION					

TOLERENCE UNLESS OTHERWISE SPECIFIED

0 MM~8 MM	±0.1
8 MM~25MM	±0.15
25MM~80MM	±0.2
80MM~250MM	±0.3
250MM~ABOVE	±0.6
ANGULAR:	±1°

KAWA ELECTRONIC R & D CENTRE

MATL.

FINISH

TITLE LCT42AEAIA1CS-A01

MODEL NO. LCT42AE

A2 PART NO. EXP-L42AE04-01

DWG. NO. L42AEEXP4

SCALE NIL | QTY. | SHEET 1 OF 1

Spare part list for LCT42Z6TA

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
	LCT42AEAIA1CS-A01	AKAI LCT42AE(LCT42Z6TA) S-MT8206 CMO (V420H1-L05 V2.2) HORIZONTAL AC120/60HZ USA SILVER/BLACK			
1>	510-L42AE02-02AK	HORIZONTAL CARTON BOX AKAI LCT42Z6TA S-MT8206 W/PHOTO CARD USA K	1.000000	Piece	K
2>	580-L42AE2B-01AP	IB E FOR AKAI LCT42Z6TA TV+ATSC NO PIP CMO MTK8206 USA	1.000000	Piece	K
3>	E3407-081001	CORD FFC P0.5 50P L=110 B-0.5-50X110-4 (8)X4(8)-0.3X0.035	1.000000	Piece	K
4>	E7501-056108	REMOTE CONTROL K001 "AKAI" 44KEYS MT8206 LCT37" (W/O DVD) USA BLACK	1.000000	SET	K
5>	E7801-P02004	PCB ASSY PSU BOARD MEGMEET MLT198L FOR 42"LCD AC110-240V OUTPUT 5V/12V/24V/5VSB 300W	1.000000	SET	K
6>	771EL42AE02-01	MAIN PCB ASS'Y S-MT8206 FOR LCT42AE CMO USA	1.000000	SET	K
7>	771S42D102-02	ATSC TUNER PCB ASS'Y (MT5111CE) W/O MAX3232	1.000000	SET	K
8>	200-L42AE01-02AA	CABINET FRONT MATT BLACK/SILVER LCT42Z6TA CMO USA A	1.000000	Piece	S
9>	202-L42AE03-01AA	CABINET BACK BLACK W/O DVD/POWER SWITCH LCT42AE FOR CMO	1.000000	Piece	S
10>	269-42SD01-01L	REMOTE RECEIVE LENS	1.000000	Piece	S
11>	310-041204-01V	POLYBAG 4"X12"X0.04 AV	1.000000	Piece	S
12>	310-111404-07V	POLYBAG 11"X14"X0.04 FV	1.000000	Piece	S
13>	310-504004-01	POLYBAG EPF 50"X40"X0.04	1.000000	Piece	S
14>	370-42D102-01	PAD CORD SPONG FOR SPK	1.000000	Piece	S
15>	426-L37AD02-01S	AC JACK BRACKET	1.000000	Piece	S
16>	436-L32AB0G-01S	TERMINAL SHEET FOR COMPONENT X2	1.000000	Piece	S
17>	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1.000000	Piece	S
18>	483-L32AB32-01S	SHIELDING COVER	1.000000	Piece	S

19>	521-550155-01	FELT PAPER 550X15X0.5MM W/ADHESIVE	2.000000	Piece	S
20>	521-950155-01	FELT PAPER 950X15X0.5MM W/ADHESIVE	2.000000	Piece	S
21>	522-421D01-01	MASKING PAPER	1.000000	Piece	S
22>	530-060035-05	FIBER WASHER 6X3.5X0.5MM W/ADHESIVE	1.000000	Piece	S
23>	553-002007-25A	SHIELD GASKET 20X7X2.5MM W/ CONDUCTIVE ADHESIVE	1.000000	Piece	S
24>	560-L42AE01-02AP	MODEL LABLE AKAI LCT42Z6TA S-MT8206 USA P	1.000000	Piece	S
25>	563-119-	SERIAL NO. LABEL	1.000000	Piece	S
26>	568-P46T02-02	WARNING LB ENG 42SF NIL	1.000000	Piece	S
27>	578-L37AD01-01AP	FUNCTION SHEET FOR TERMINAL LCT37" S-MT8202 USA P	1.000000	Piece	S
28>	579-42D102-09	SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
29>	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
30>	579-L27AD09-01	CAUTION LABEL ENG AKAI	1.000000	Piece	S
31>	579-L32AD09-02AP	FCC STATEMENT LABEL 77X20MM	1.000000	Piece	S
32>	579-L42AE01-02AP	BAR CODE LABEL AKAI LCT42Z6TA USA	2.000000	Piece	S
33>	590-L42AE01-02AP	WARRANTY CARD AKAI ENG LCT42Z6TA USA P	1.000000	Piece	S
34>	593-L42AE01-02AP	INSERTION CARD AKAI ENG LCT42Z6TA USA P	1.000000	Piece	S
35>	599-L42AE01-01BP	IB SHEET E FOR LCT42AE STAND(BP04) USA(RS)	1.000000	Piece	S
36>	599-L42AE02-01AP	IB SHEET E FOR LCT37AE/LCT42AE INITIAL SETUP USA	1.000000	Piece	S
37>	E3404-157004	AC CORD UL 1.88M (YY-3/ST3 YUNBIAO)	1.000000	Piece	S
38>	E3421-925118	WIRE ASSY 8P2.5/7P2.0 L170MM 5V 12V SIGNAL POWER MT8202	1.000000	Piece	S

Spare part list for LCT42Z6TA

39>	E3421-925127	WIRE ASSY TJC3-2Y L860 SPK-R MT8202	1.000000	Piece	S
40>	E3421-925139	WIRE ASSY TJC3-3Y L760MM LCD37" MT8202 SPK-L	1.000000	Piece	S
41>	E3421-925153	WIRE ASSY 250MM 3WIRES 20# 1617 FOR POWER IN PUT	1.000000	Piece	S
42>	E3421-925230	WIRE ASSY 9P396P11P2.5/10P/2.5/7P/2.54P/2.5	1.000000	Piece	S
43>	E3461-000125	WIRE INVERTER 14P2.0/10P2.5/3P2.0 L=700MM/400MM	1.000000	Piece	S
44>	E3461-000126	WIRE INVERTER 12P/2.0/10P/2.5 L350MM LCD42" (SUB INVERTER)	1.000000	Piece	S
45>	E3471-000075	WIRE WS SHIELD F1-R51S-H L300MM LCT37&47 CMO MT8202 LVDS NEW	1.000000	Piece	S
46>	E3471-000085	WIRE WS SHIELD WIRE LCT42" FOR MT8206 KEY	1.000000	Piece	S
47>	E4801-135001	SPEAKER 8 OHM 12W D3" SG78F801	2.000000	Piece	S
48>	E6203-42CD02	DISPLAY LCD 42" CMO WXGA V420H1-L05	1.000000	Piece	S
49>	E7301-010002	BATTERY AAA R03P1.5V <2>	2.000000	Piece	S
50>	G300-L42AE13-02CA	ROHS POLYFOAM BOTTOM EPS (SHANGHAO)	1.000000	Piece	S
51>	G300-L42AE14-02CA	ROHS POLYFOAM TOP EPS (SHANG HAO)	1.000000	Piece	S
52>	734-BP0403-02	PLASTIC STAND FOR 421D CD=460MM W/ PACKING EXPLODE H=270MM MATT BLACK	1.000000	SET	S
53>	771BL42AE02-01	IR RECEIVE PCB ASS'Y FOR LCT42AE S-MT8206	1.000000	SET	S
54>	771KL42AE02-01	KEY PCB ASS'Y FOR LCT42AE S-MT8206	1.000000	SET	S

Software Upgrade

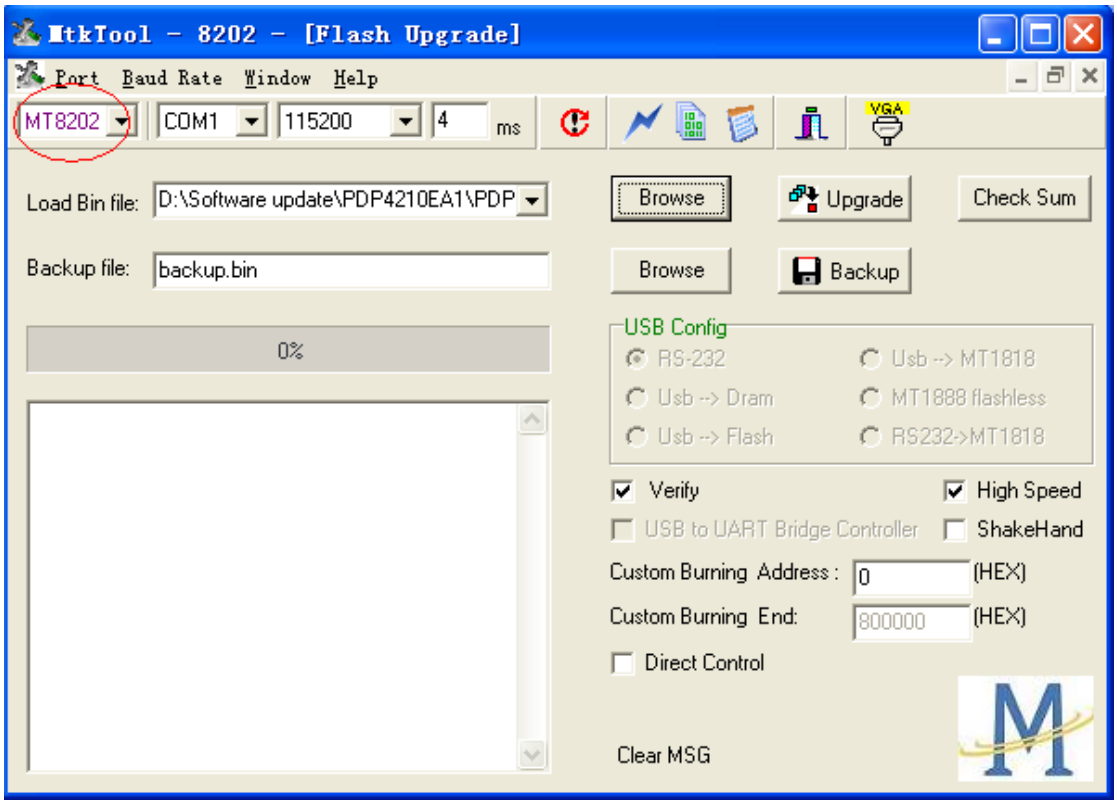
Process of update MT8202

Preparing :

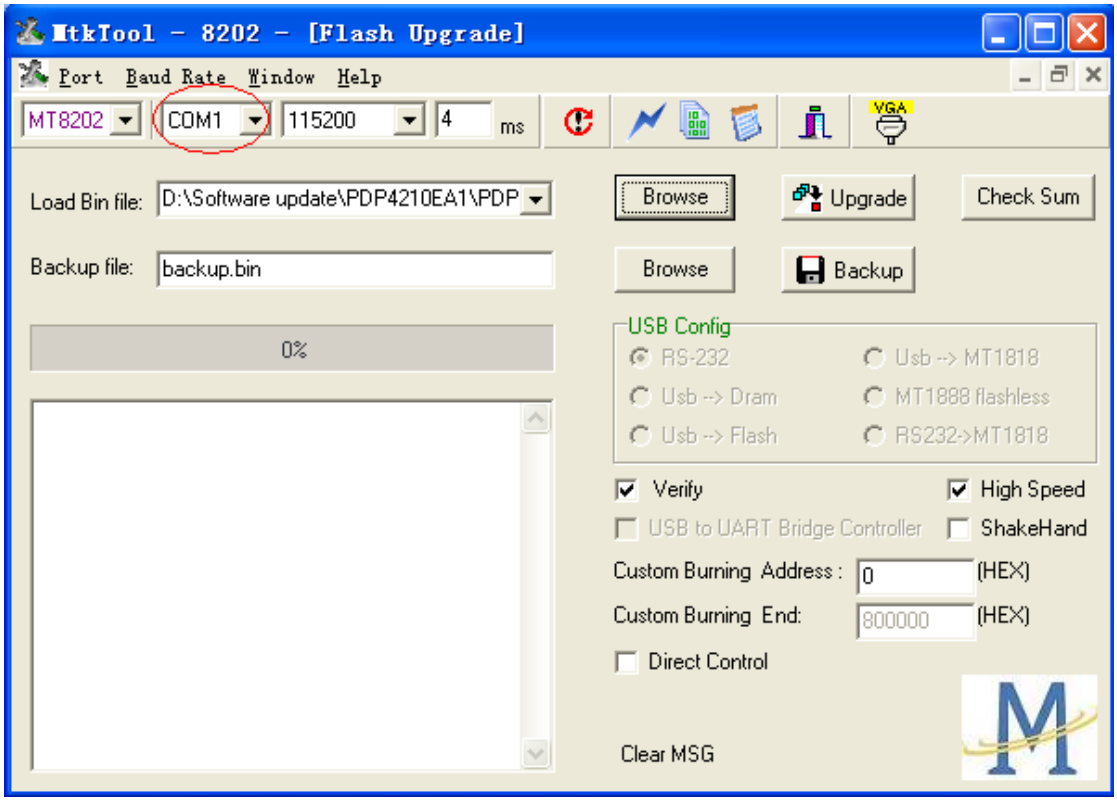
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**.Please find the details for connecting **refering to the appendix at the end of this file.**
2. Store the MtkTool into the PC .

Downloading :

3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT8202. (the software of MTKtool will be sent to your side)

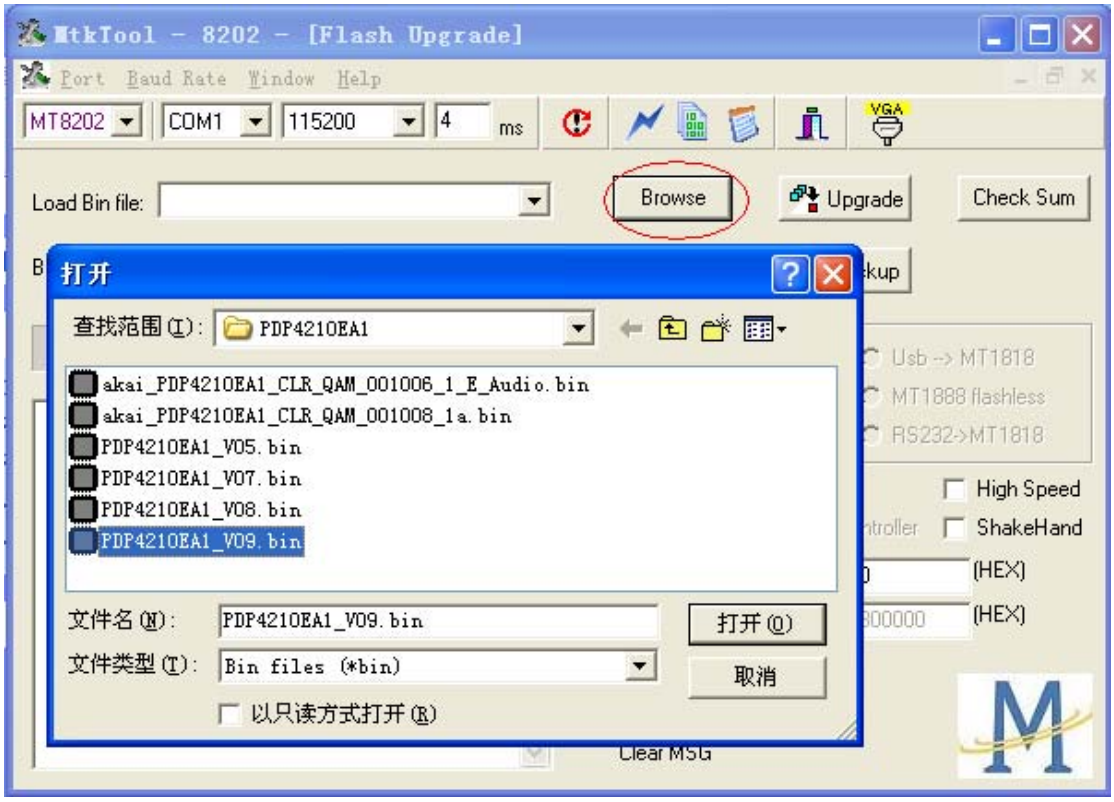


5. Select current COM port. (please try to check the COM port of your PC).

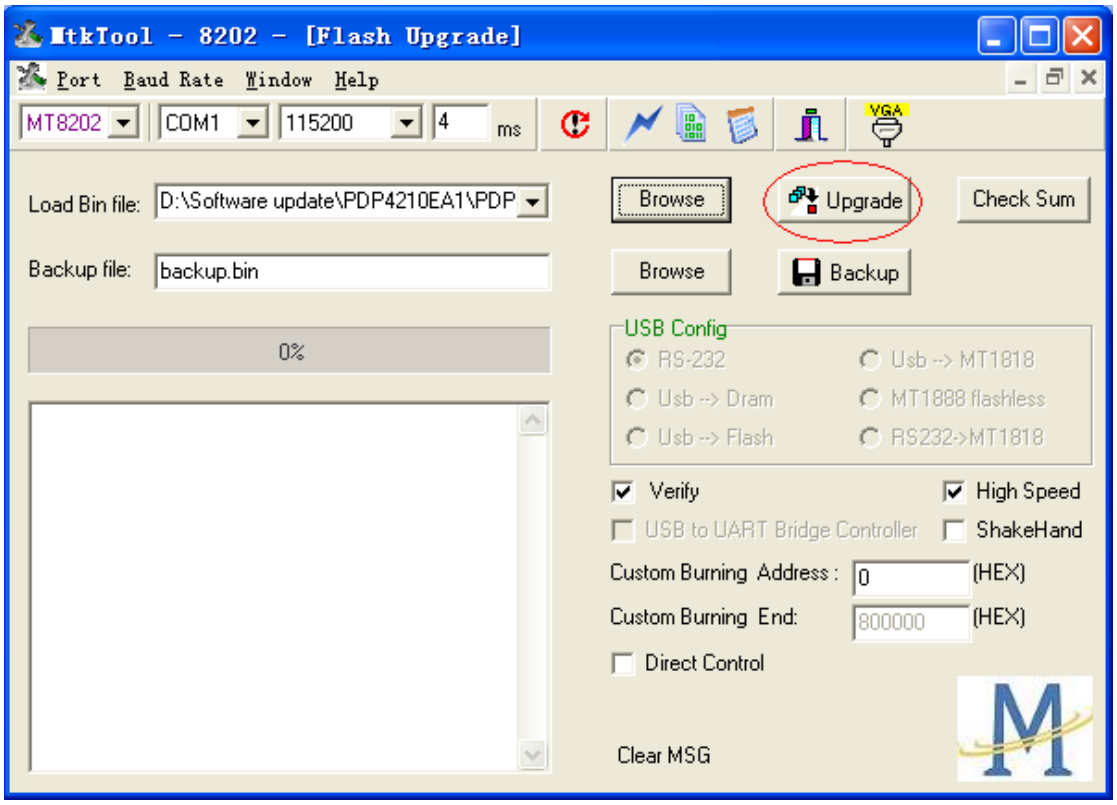


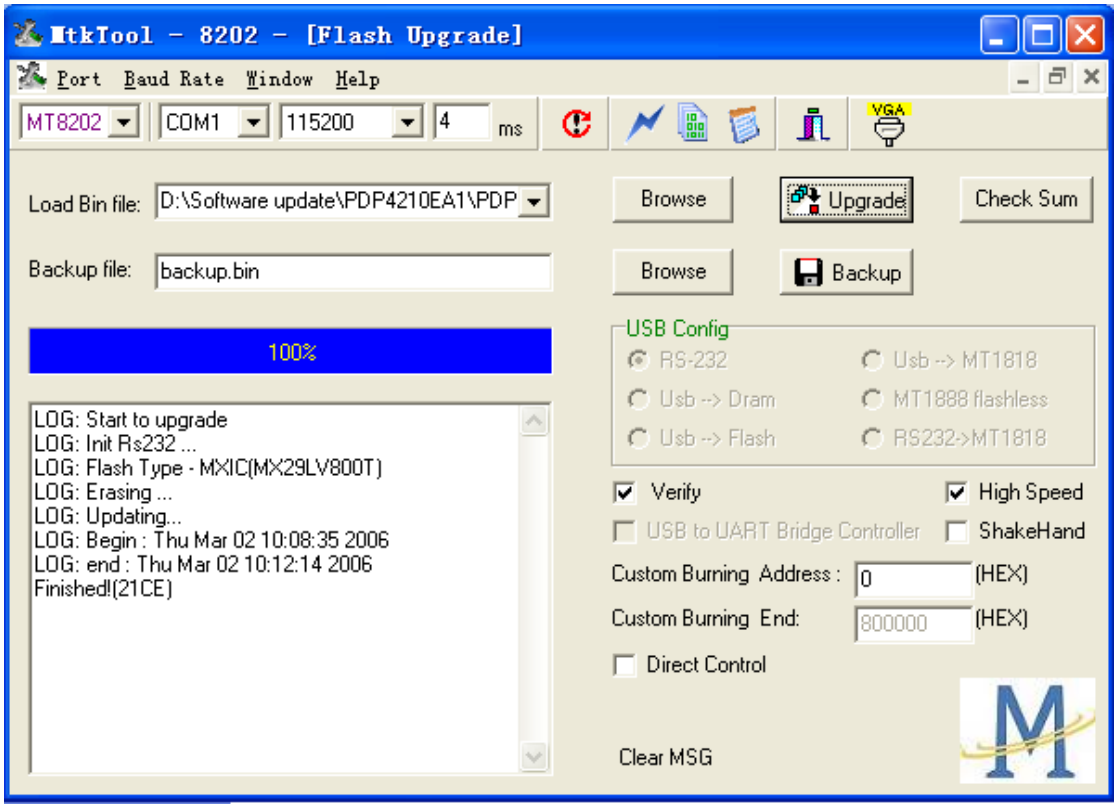
6. Choose the bit rate as 115200.

7. Select the update binary by pressing browse button. For example,the binary file name is PDP4210EA1_V09.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.





9. The update process is successful as the progress bar is 100%. After the update process is ok,

turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT8202 which has been download into the Plasma TV .

Press Menu button of the remote control，following input “8202”of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the mode of Firmware Version and then enter the mode of Firmware Version . It is easy to be found the version of the current firmware for MT8202 is as the following : “Factory ID : PDP4210EA1_VXX ”

Appendix:

Quick Installation Guide

For

Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

2. Installation for ATV upgrade

2.1 Connect RS232 cable (#2) to PC serial port

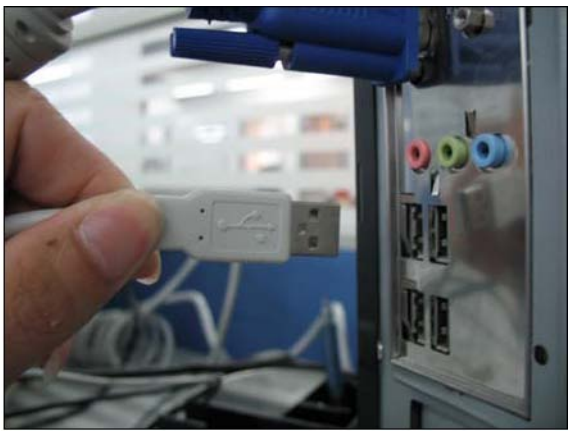
Connect another side of RS232 cable (#2) to the board (#1)

2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)

Connect RS232-VGA cable (#4) (VGA side) to the TV

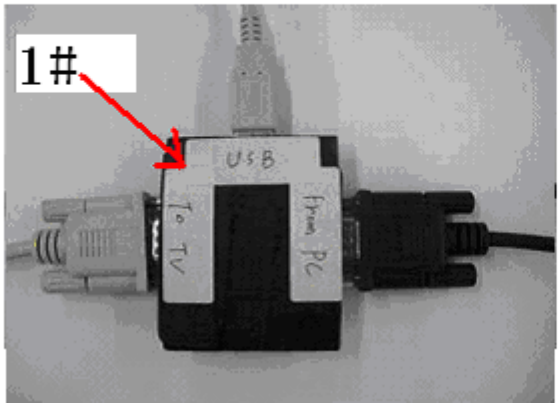
2.3 Connect USB cable (#5) to the board (#1)

Connect another side of USB cable (#5) to PC

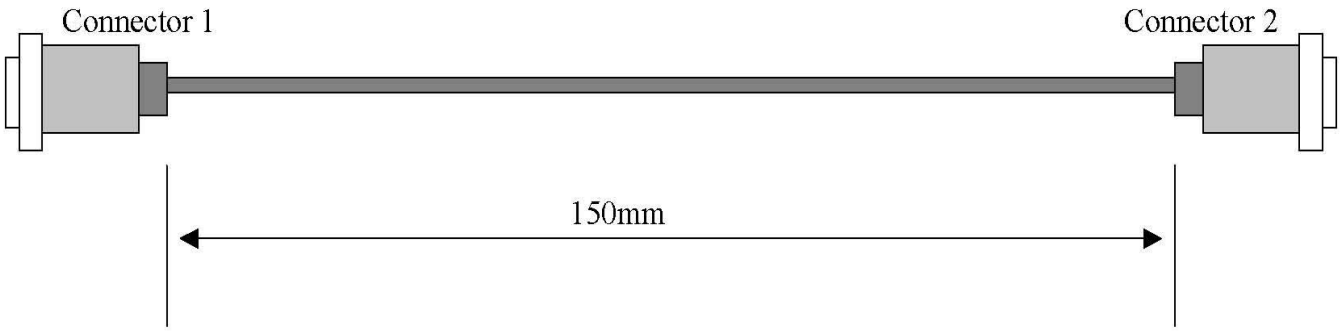


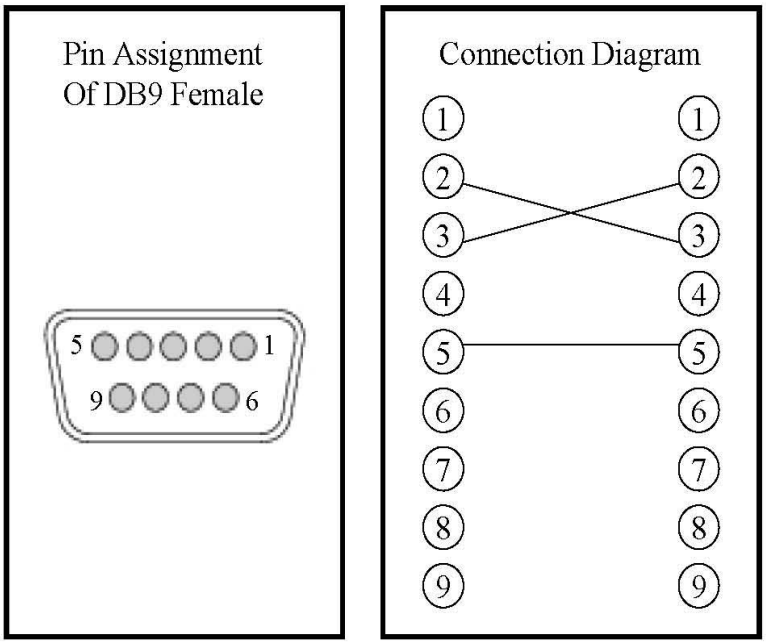
3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



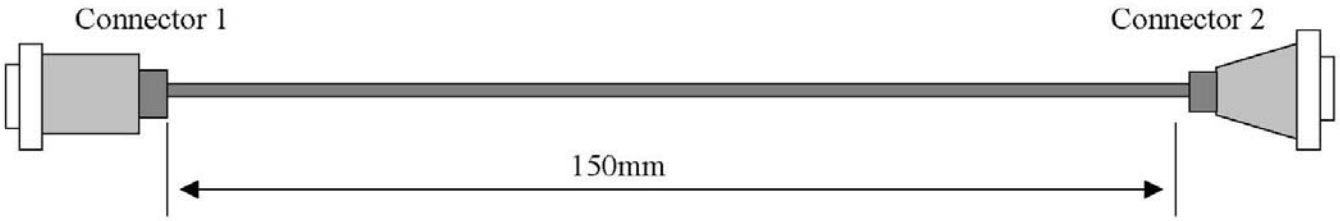
RS232 Null Cable for PC (#2)

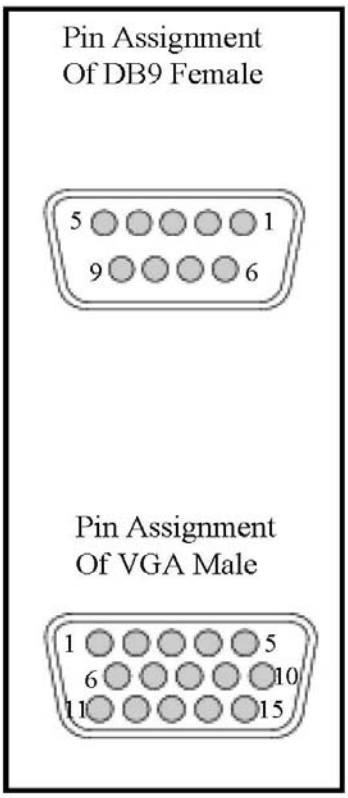


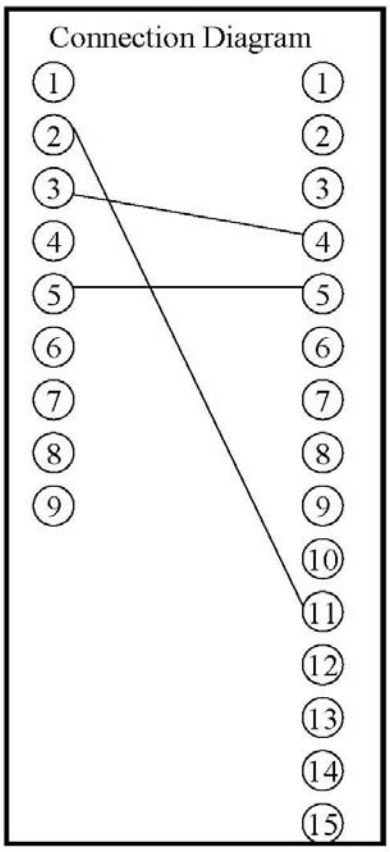


Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 - VGA Cable (#4)

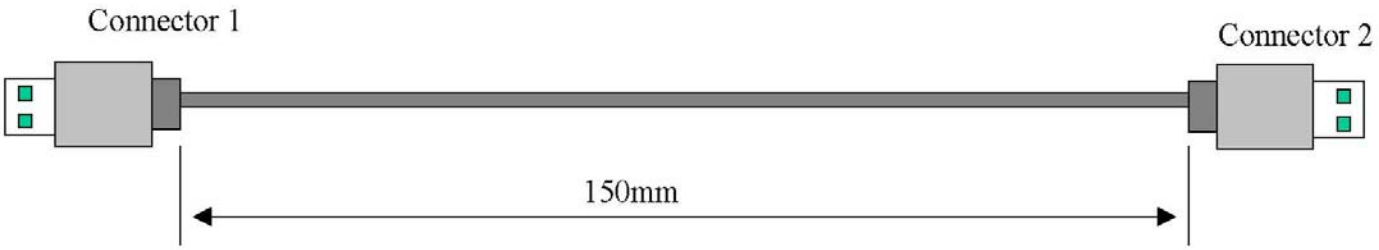






Connector 1: DB9 Female
Connector 2: VGA Male

USB Cable (#5)



Connector 1: Standard USB Male
Connector 2: Standard USB Male

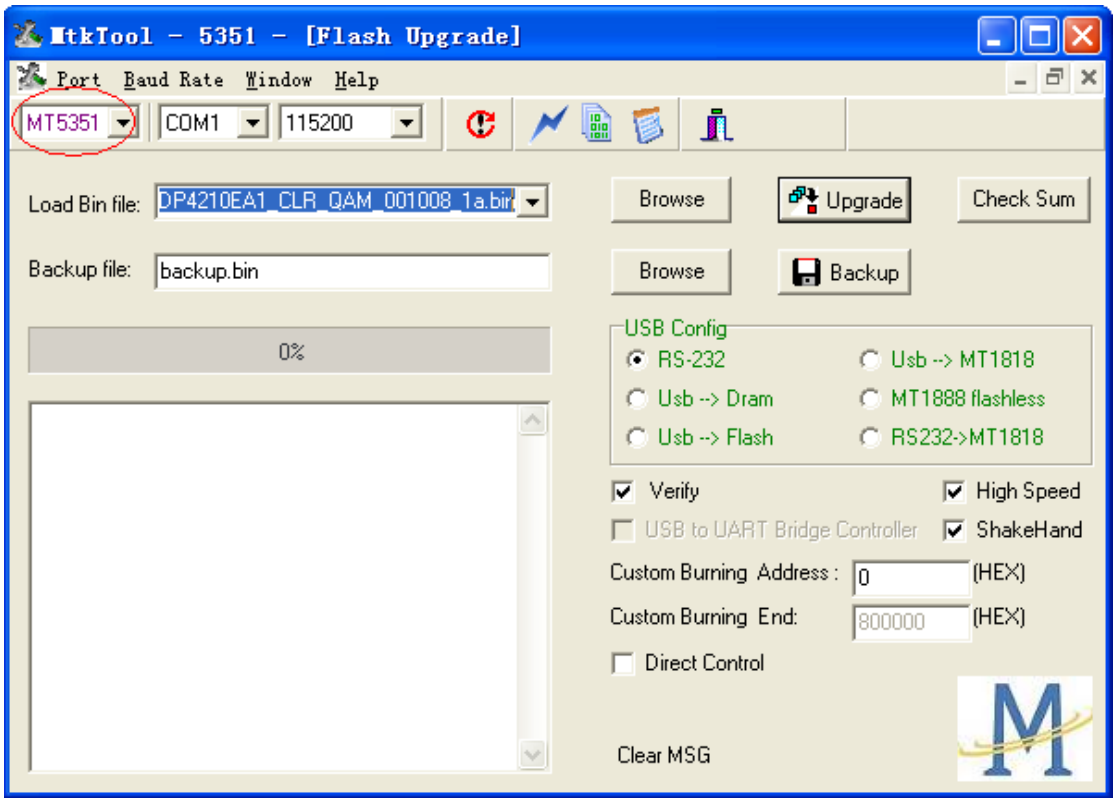
Process of update MT5351AG

Preparing :

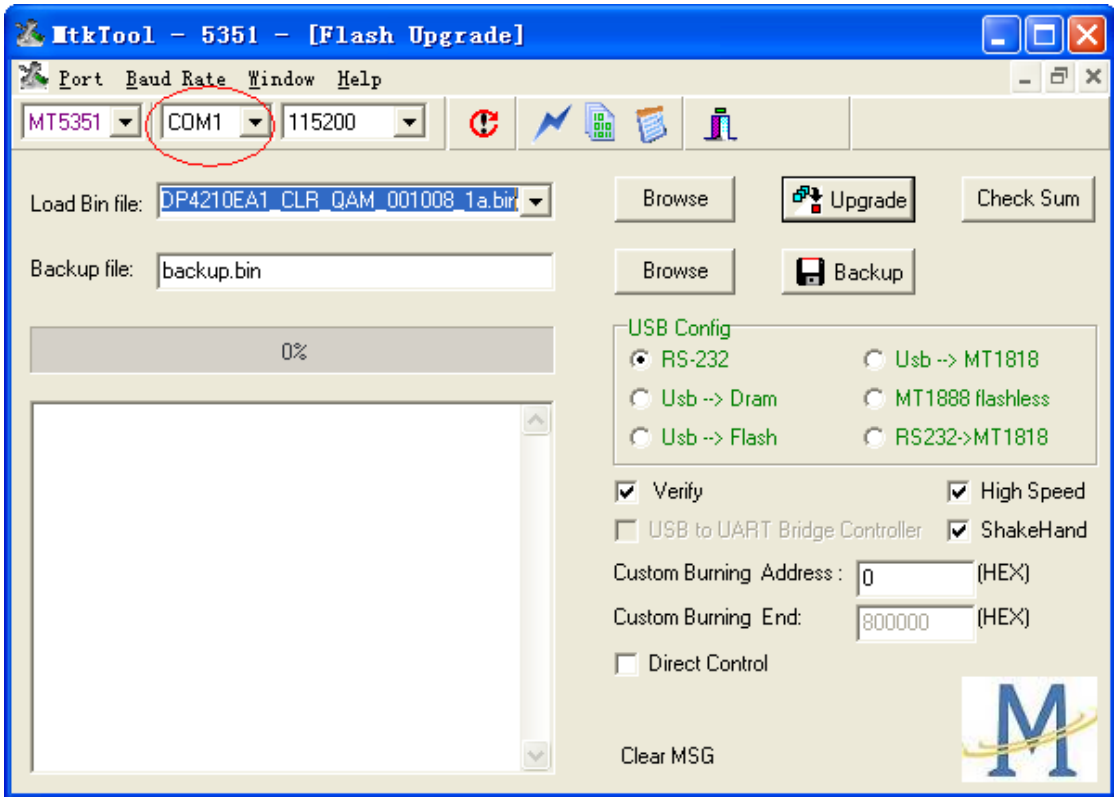
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**.Please find the details for connecting **refering to the appendix at the end of this file.**
2. Store the MtkTool into the PC

Downloading :

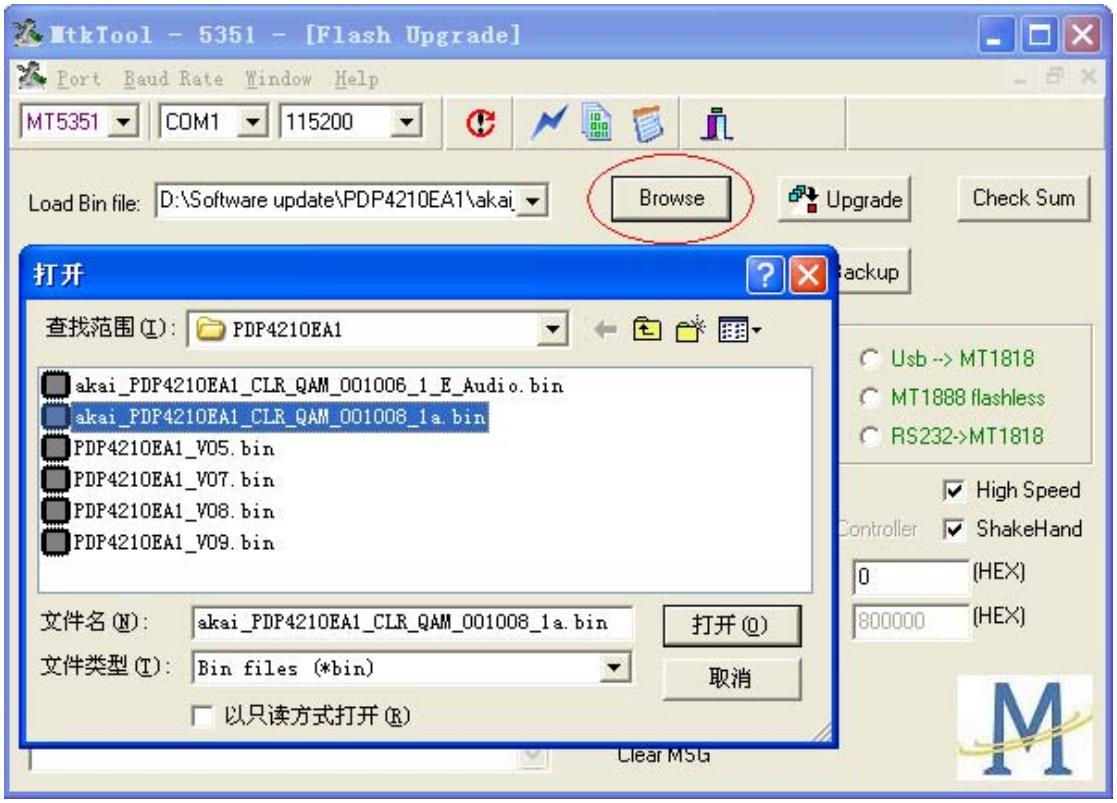
3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT5351. (the software of MTKtool will be sent to your side)



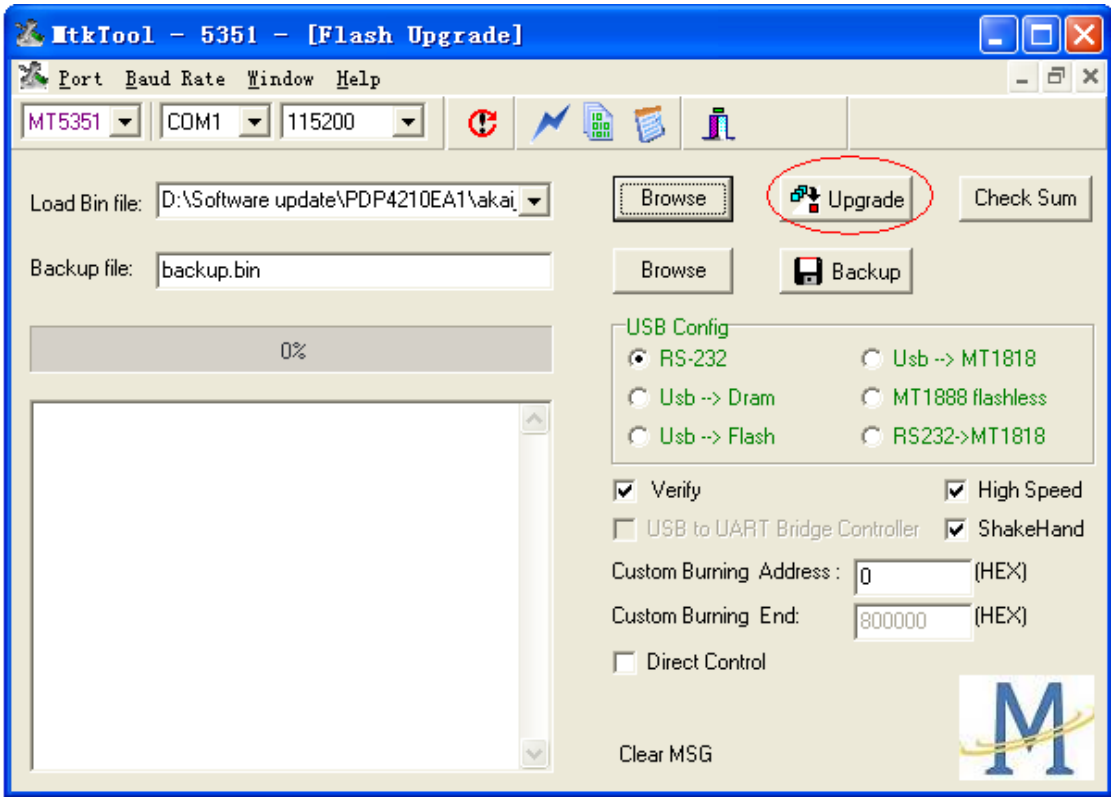
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example,the binary file name is XXXX_PDP4210EA1_000000XX_X_P.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking :

It is needed to check the version of the firmware for MT5351AG which has been download into the Plasma TV .

Press Menu button of the remote control and the main OSD menu is appeared on the screen .

Use the remote control and select the DTV menu . following input “0000” (zero , zero , zero , zero) of the remote control .Then enter the mode of factory after input the digits .

It is easy to be found the version of the current firmware for MT5351AG is “PDP4210EA1 CLA_QAM_XXXXXX_XX”under the mode of factory .

Appendix:

Quick Installation Guide

For

Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 null cable x 1 for DTV (#3)
- USB cable x 1 (#5)

2. Installation for DTV upgrade

2.1 Connect RS232 cable (#2) to PC serial port

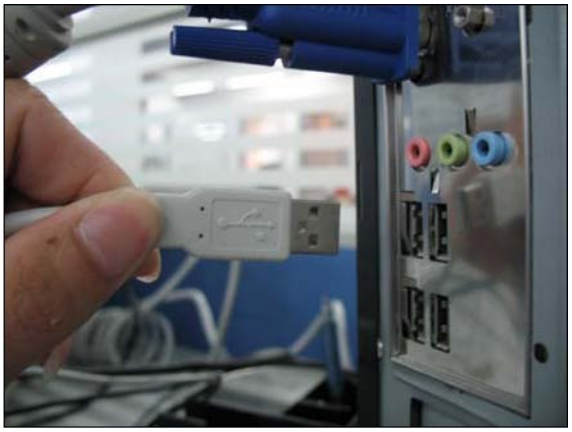
Connect another side of RS232 cable (#2) to the board (#1)

2.2 Connect RS232 cable for DTV (#3) to the board (#1)

Connect another side of RS232 cable for DTV (#3) to the TV

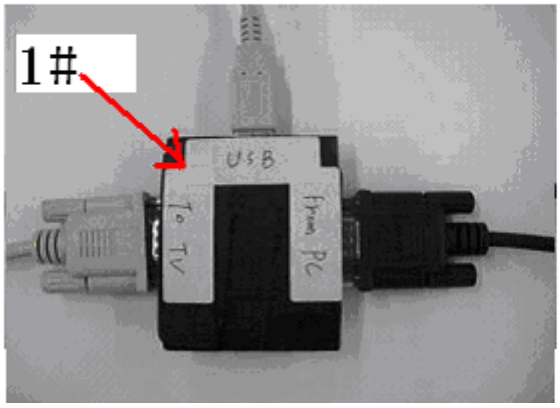
2.3 Connect USB cable (#5) to the board (#1)

Connect another side of USB cable (#5) to PC

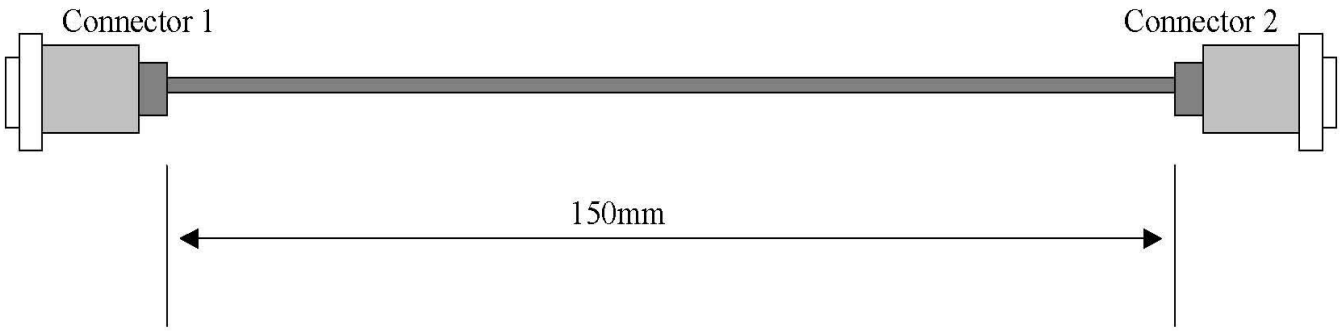


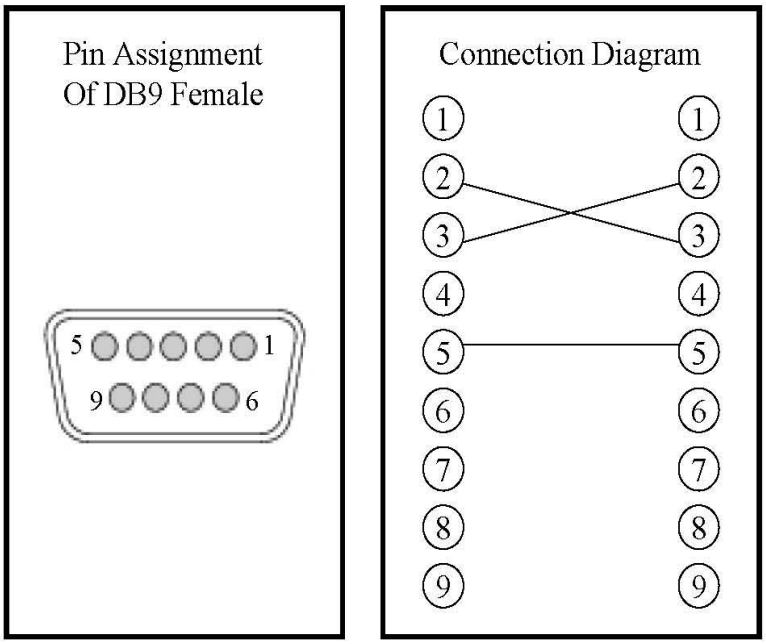
3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



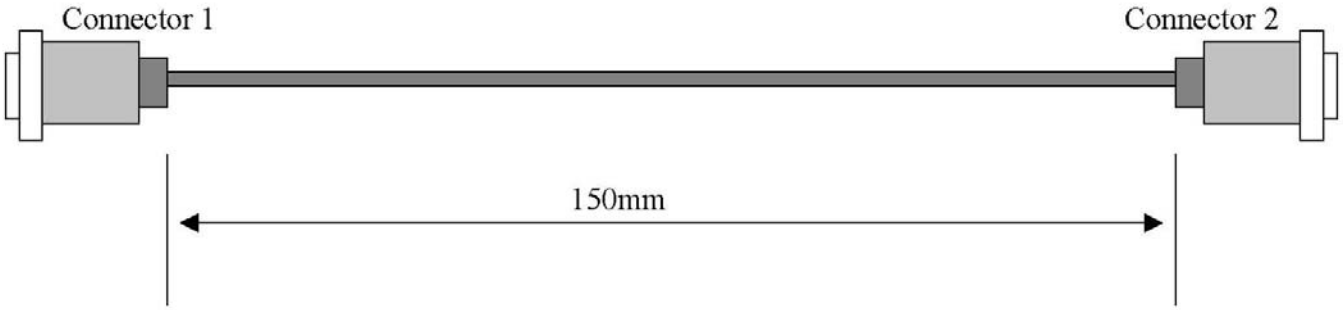
RS232 Null Cable for PC (#2)

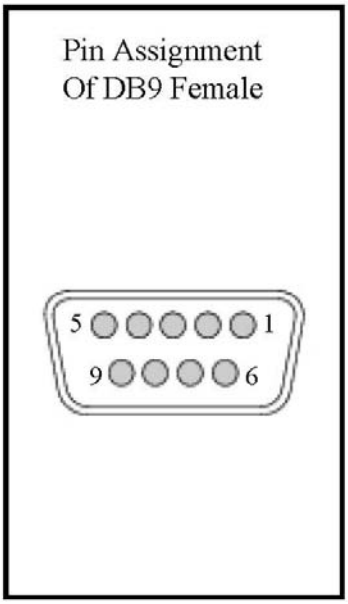


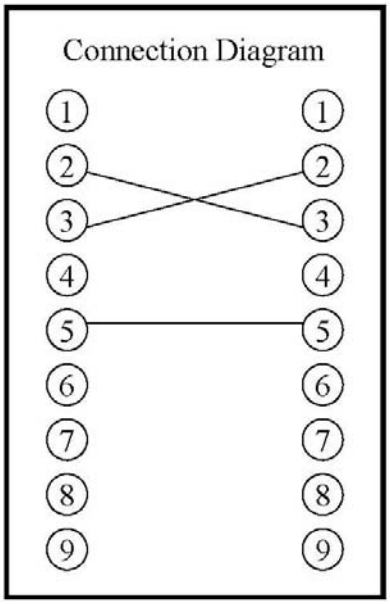


Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 Null Cable for DTV (#3)

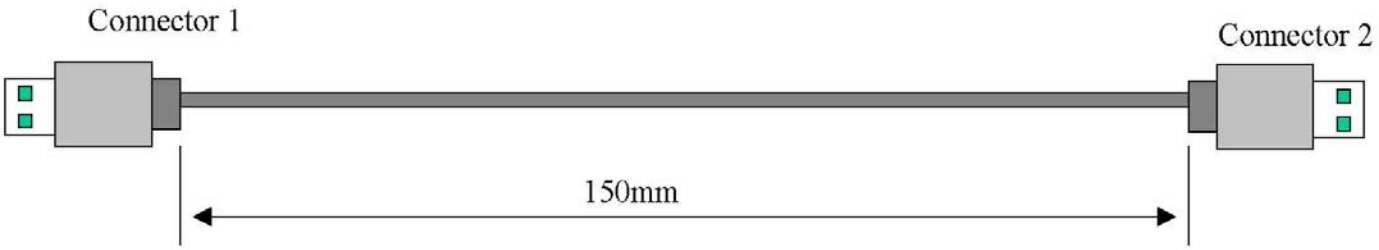






Connector 1: DB9 Female
Connector 2: DB9 Female

USB Cable (#5)



Connector 1: Standard USB Male
Connector 2: Standard USB Male